HCAL Front End Electronics

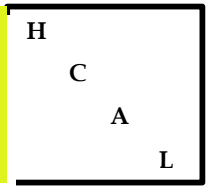
Theresa Shaw

CMS HCAL Electronics Project Engineer

CMS Electronics Week

May 18, 2001

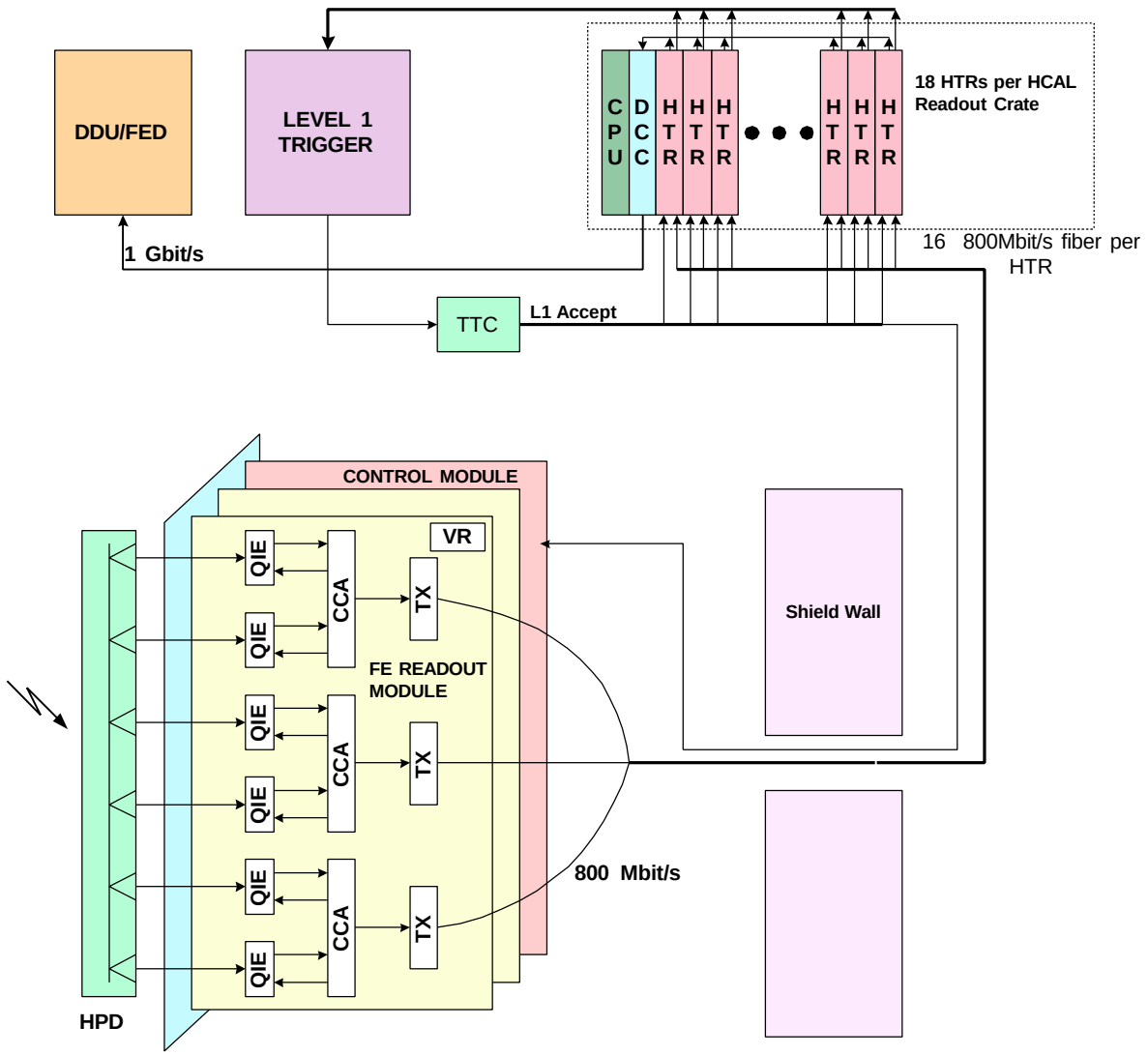
Electronics Overview



Electronics

- System Overview
- Packaging
- Power
- Backplane
- Readout Module (RM)
- ASICs

FE/DAQ Readout



Packaging

HB, HE, and HO will be packed in custom Readout BoXes (RBX)

HF will be packed in standard Eurocard Crates

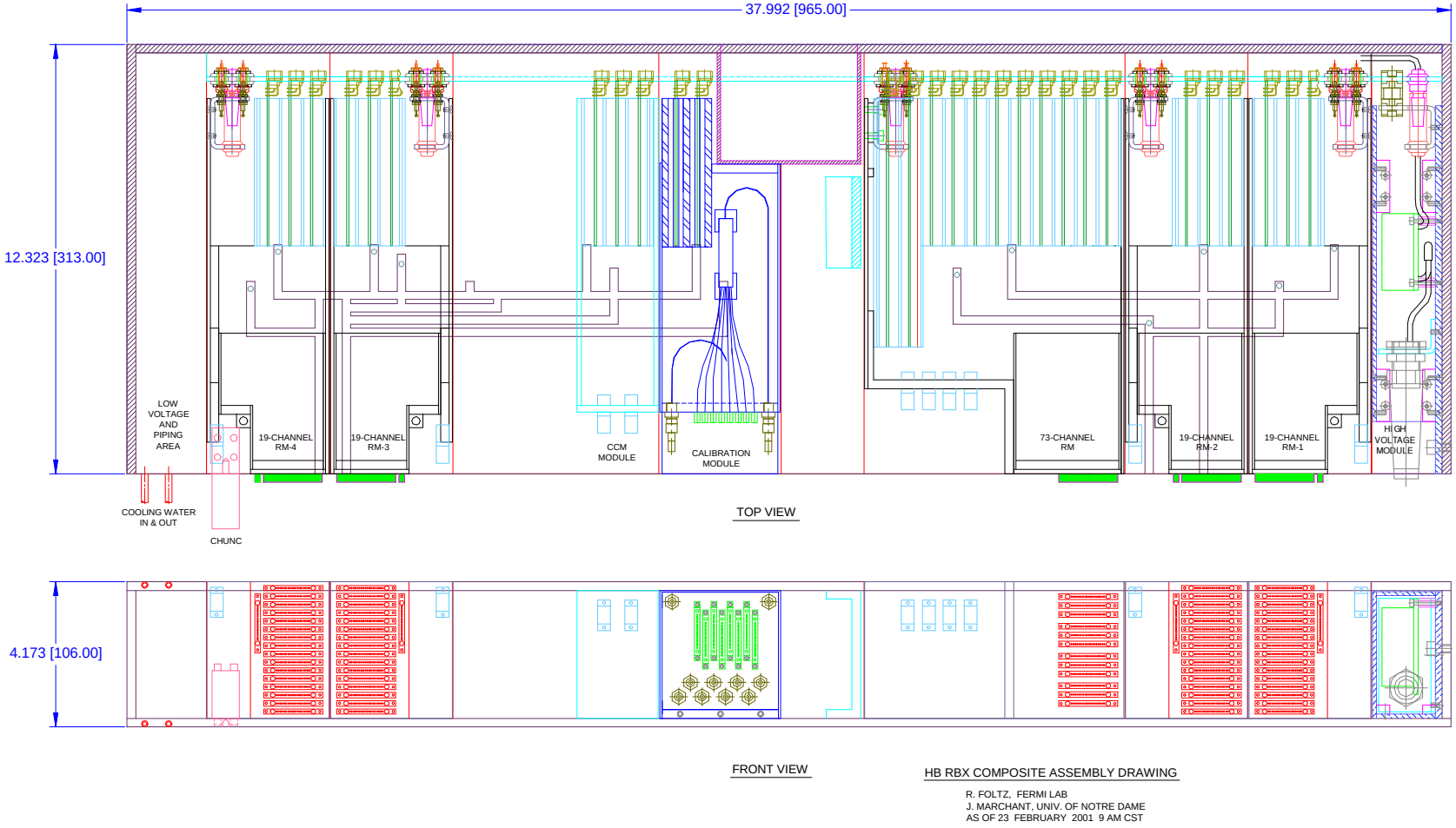
Crates Provide

- **Power**
- **Cooling**
- **Clock distribution**
- **Slow Controls Communication**

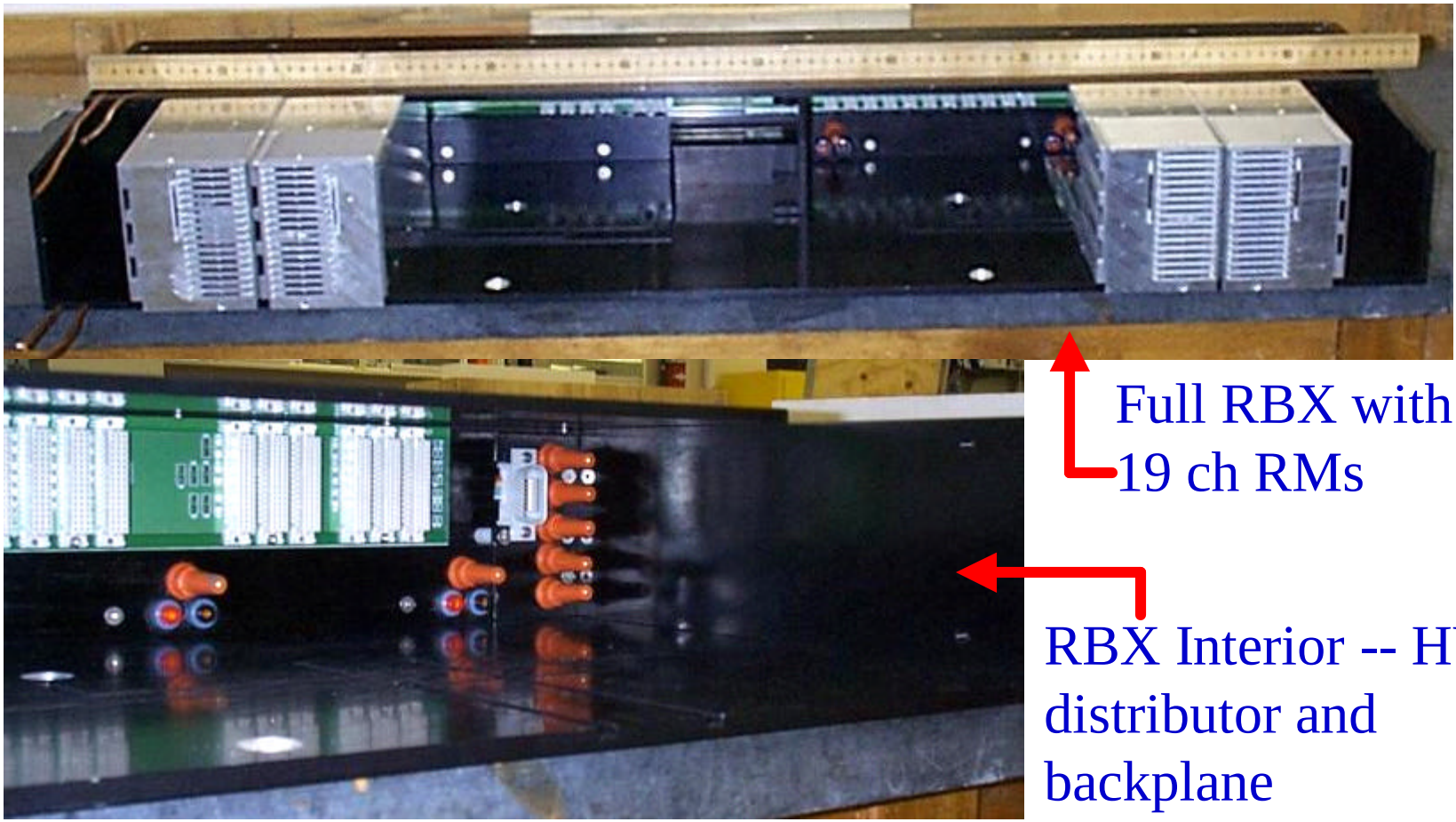
HB RBX

36 HB RBXs

4968 Channels



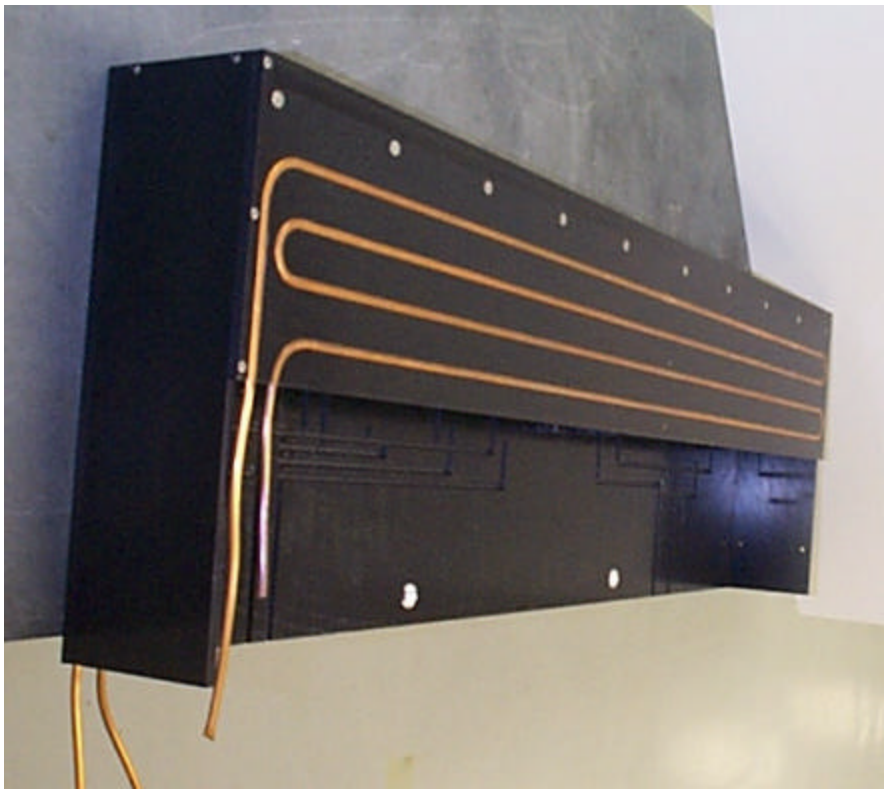
HB RBX Assembly



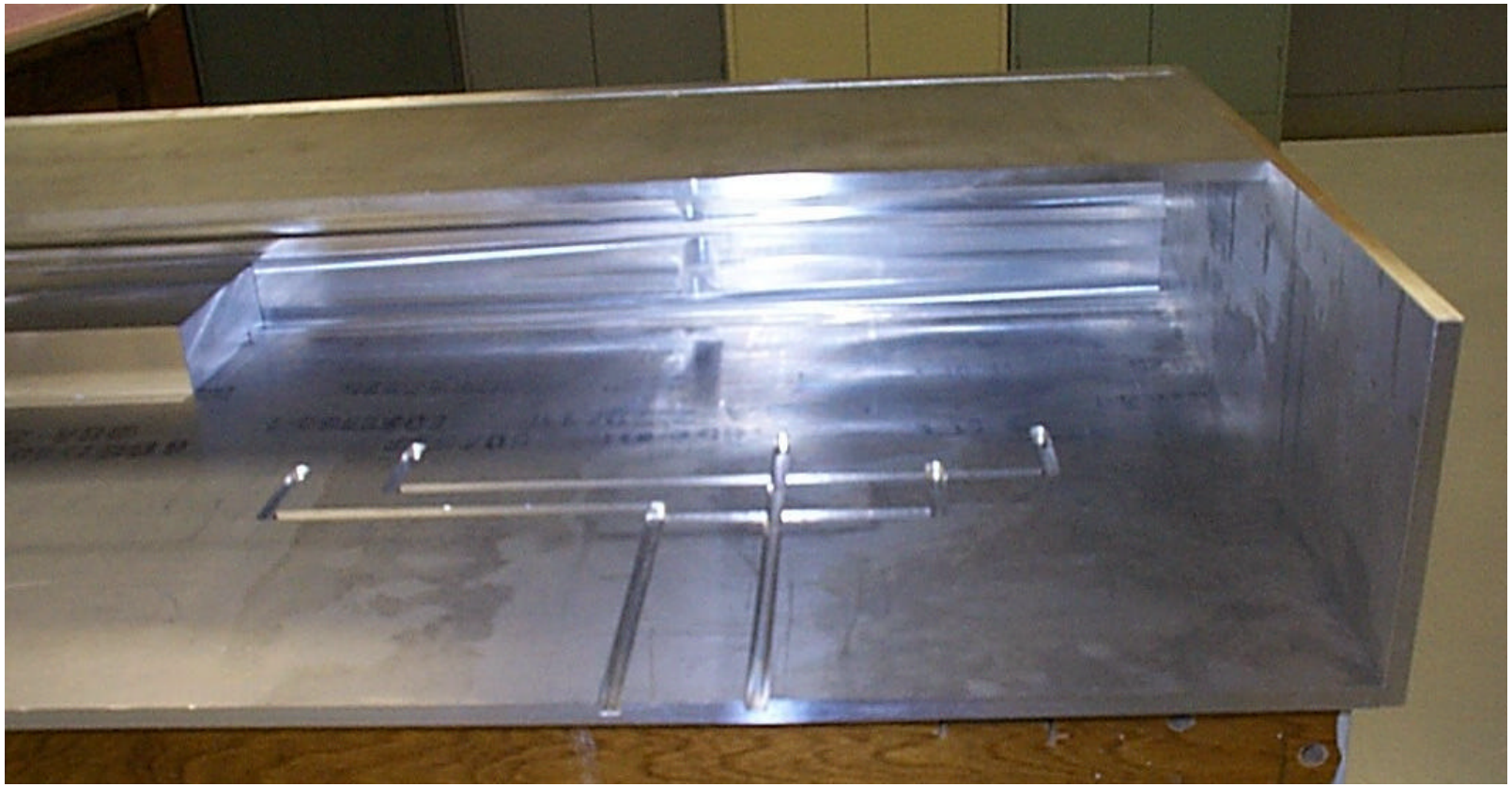
Full RBX with 19 ch RMs

RBX Interior -- HV distributor and backplane

Cooling Routing on RBX enclosure outer surface



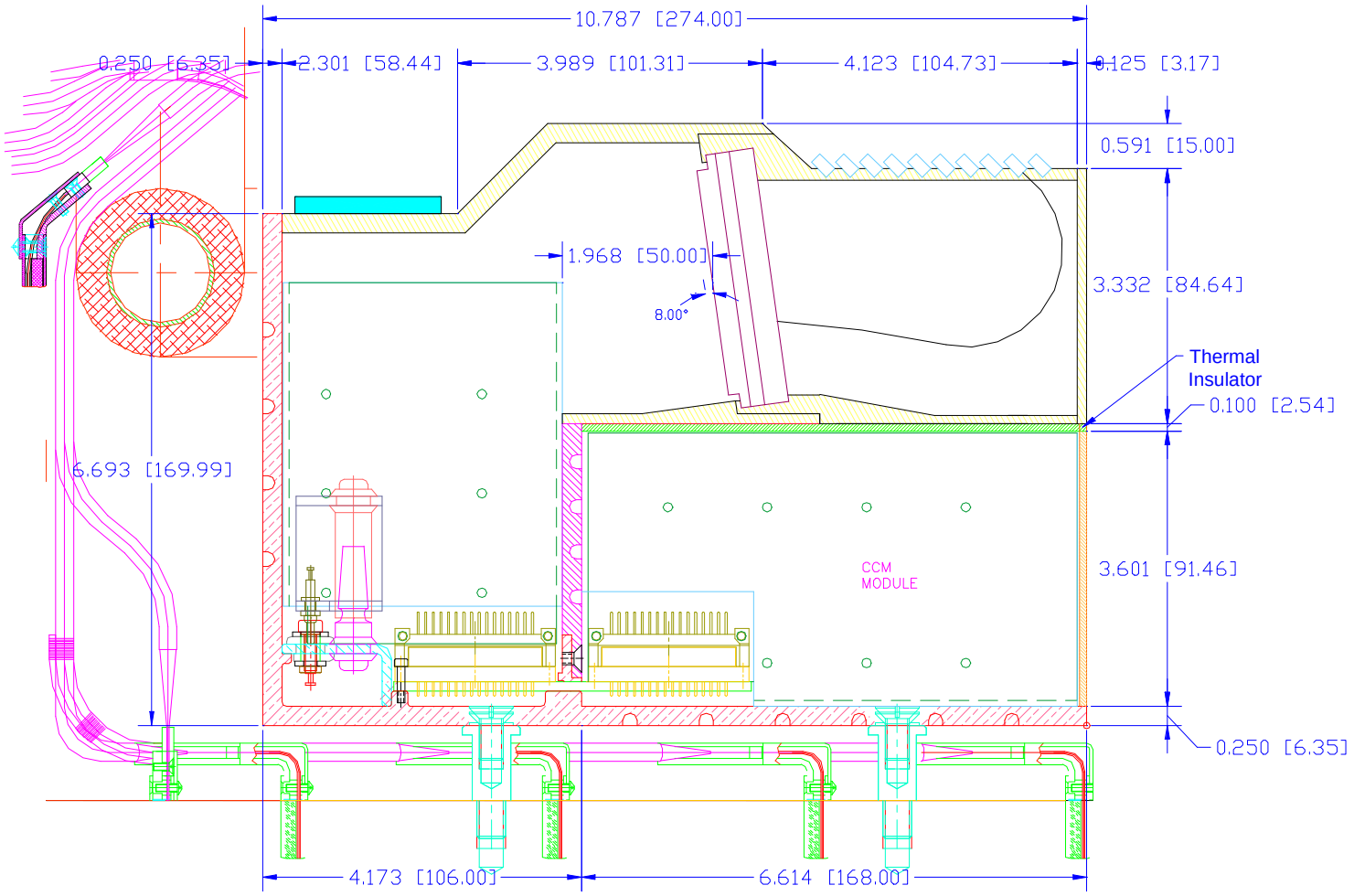
HB RBX Module Routing Channels



HE RBX (r,z) view

36 HE RBXs

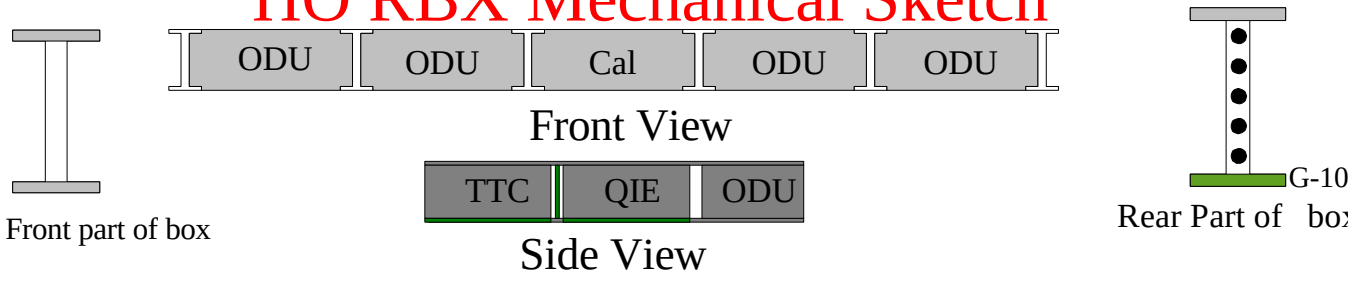
3672 Channels

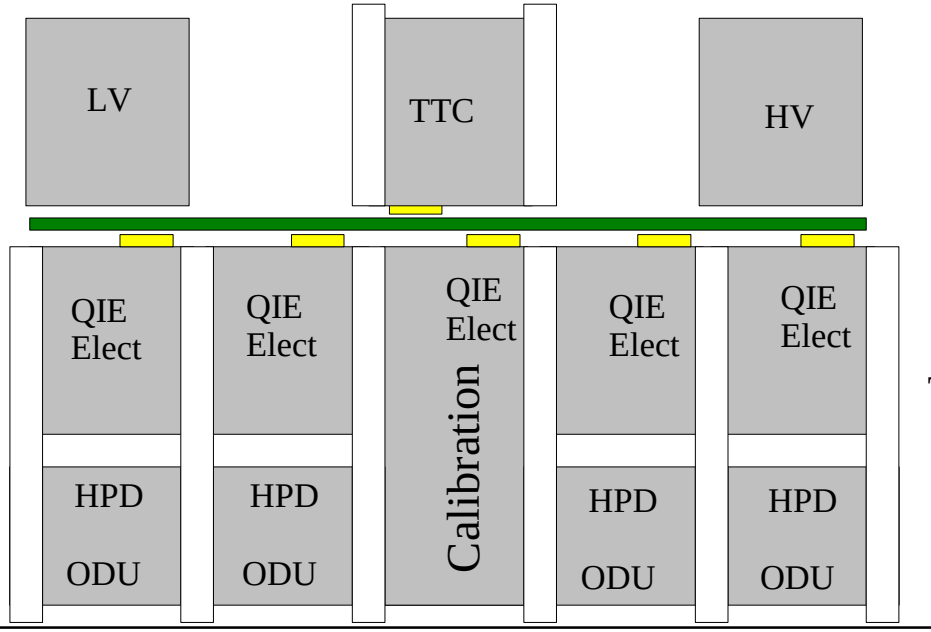


HO RBX Concept

36 HO RBXs **3744 Channels**

HO RBX Mechanical Sketch





TOP View

HF Channel Count

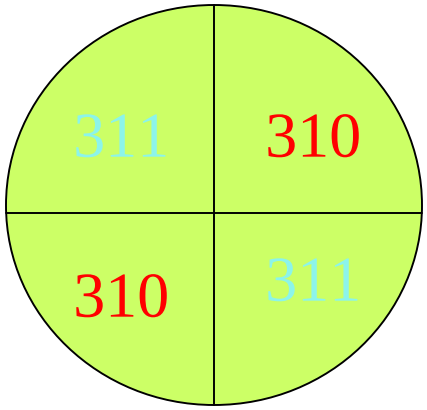
2484 Channels (includes “ECAL” & “TC”)

1242 Channels per end

310 ½ Channels per quadrant
(4 crates on each end)

51 3/4 Readout cards per crate
(6 QIE per card)

$311 = (5\times35)+(4\times34)$

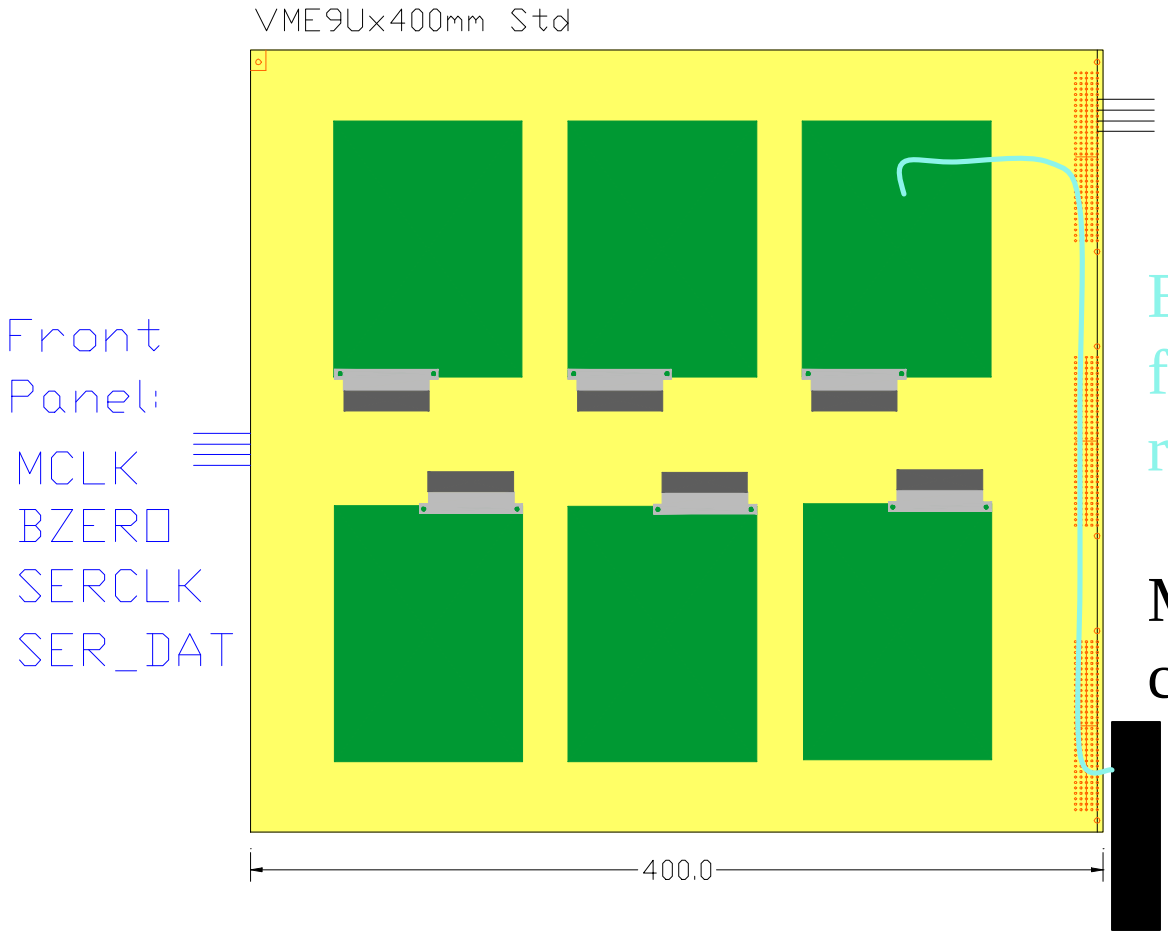


$310 = (4\times35)+(5\times34)$

$\Rightarrow$ need 52 Readout cards per crate

HF 9U Packaging Proposal

6x6=36 channels



External coax cabling from PMT input to readout card (36 total)

Multisignal microcoax connector

		BOSTON UNIVERSITY Electronics Design Facility
Drawn By:	J. Rohlf	9U VME Motherboard
		Preliminary HF Readout
		FILENAME.EXT 1/30/01 REV:

HF 3U Packaging Proposal

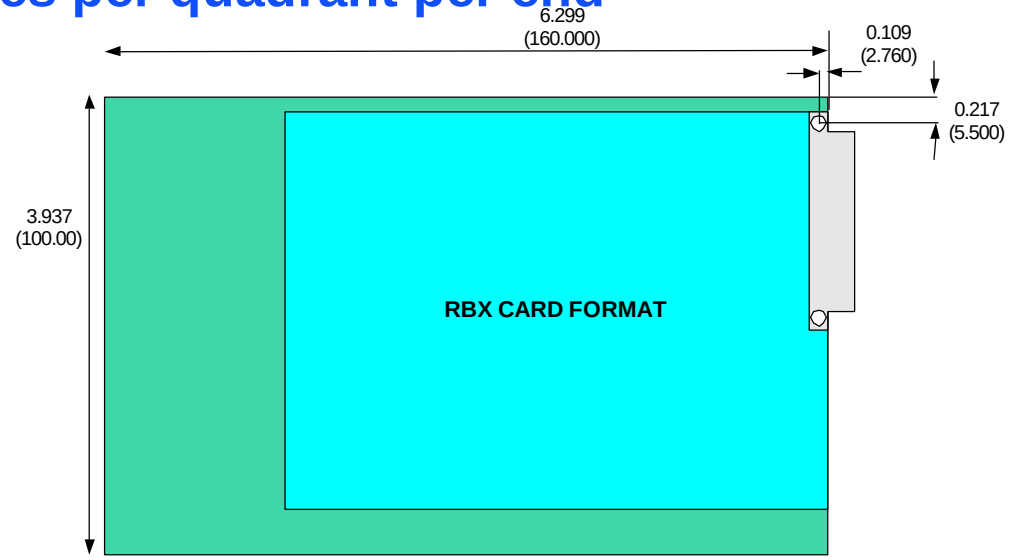
Produce Readout Cards in 3U Format

Use Commercial 3U Crate

Produce Custom Backplane (similar to HB, HE and HO)

- **18 slots for Readout Cards (108 channels)**
- **3 slots for Clock and Control Modules**

=>3 3U crates per quadrant per end



Readout Module Dimensions
3U Eurocard Format

Power Consumption

Power Consumption

HB – 298 W
23A@6.5V
33A@4.5V

HE – 205 W
17A@6.5V
21A@4.5V

HO+/- – 135 W
10A@6.5V
15A@4.5V

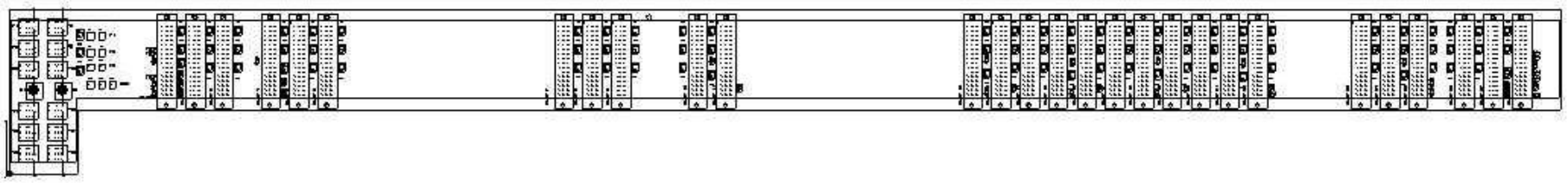
HO-0 – 189 W
16A@6.5V
21A@4.5V

			CURRENT and POWER at BOARD LEVEL										
FE Boards	QTY/BRD			POWER CONSUPTION					IDLING CURRENT				**TOTAL**
		VOLTAGE	5	5	2.5	3.3		5	5	2.5	3.3		
Chips													
QIE	6		0.2	0.4									
CCA	3					0.3							
Serializer	3				0.5								
LV regulat	3							0.025	0.025		0.025		
Current / Board			0.265	0.505		0.897727							
Total Power / Board													**9.044773**
Calibration Module		(There are two boards per module)											
		VOLTAGE	5	5	2.5	3.3		5	5	2.5	3.3		
Chips													
QIE	3		0.2	0.4									
CCA	3					0.3							
Serializer	2				0.5								
LV regulat	3							0.025	0.025		0.025		
Current / Module			0.145	0.265		0.697727							
Total Power / Module													**5.804773**
CCM													
		VOLTAGE				3.3							
Chips						5							
LV regulators													
Current / Board						1.515152							
Total Power / Board													**6.818182**

HB Backplane Function

Backplane

- ~87 CM LONG
- Provides Power
- Distributes 40 MHz Clock (3 load max)
- Provides path for RBXbus (serial communication bus)
- Temperature feedback



Backplane Low Voltage Power Connector

Product Facts

"Inverse-sex" design meets IEC 950 safety requirements

Current rated at 7.8 amperes per contact, 23.5 amperes per module, fully energized

Sequenced right-angle headers available for "make-first/break-last" applications

ACTION PIN press-fit contacts on both headers and receptacle

Contacts designed for up to 250 mating cycles

Recognized to U.S. and Canadian requirements under the Component Recognition Program of Underwriters Laboratories Inc.

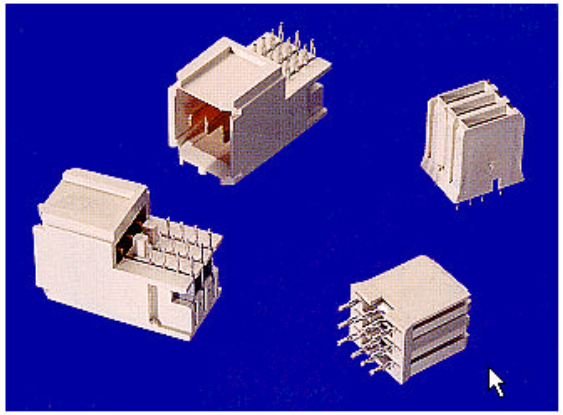
Low Voltage Distribution

3 Backplane Voltages

V1 (3 Universal Power Module Connectors for V1)
V2 (2 Universal Power Module Connectors for V2)
V3 (1 Universal Power Module Connectors for V3)
GND (6 Universal Power Module Connectors for GND)

Connectors allow for power sequencing

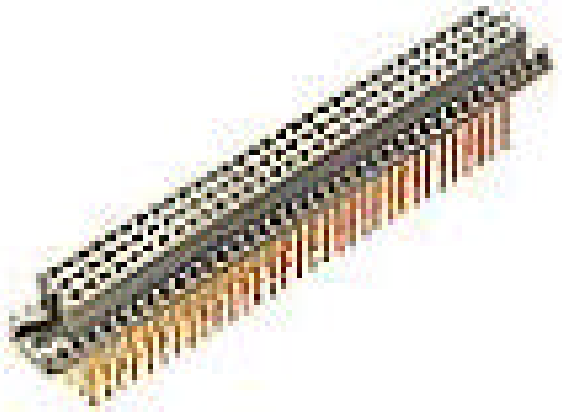
Universal Power Module



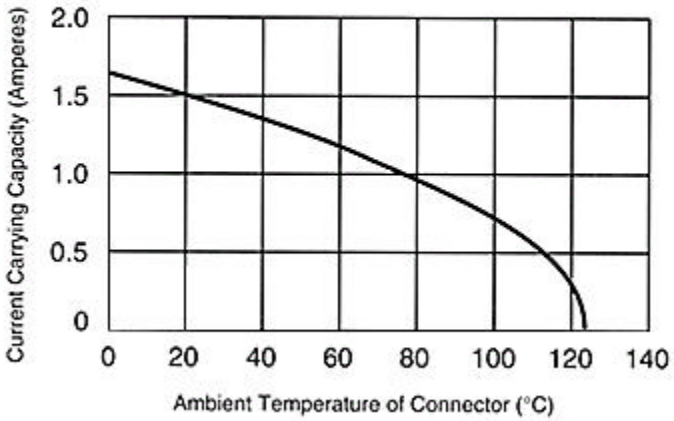
Backplane Connectors

Type C and Enhanced Type C Assemblies

Minimum adjacent mounting space required:
12.7 [.500]
Current Rating:
Per DIN 41612*
Voltage Rating:
250 VAC
Dielectric Rating:
1000 VAC
Contact Resistance:
15 milliohms initial at 100 ma and 50 mv, open circuit



Types B, C, Q and R per DIN 41612

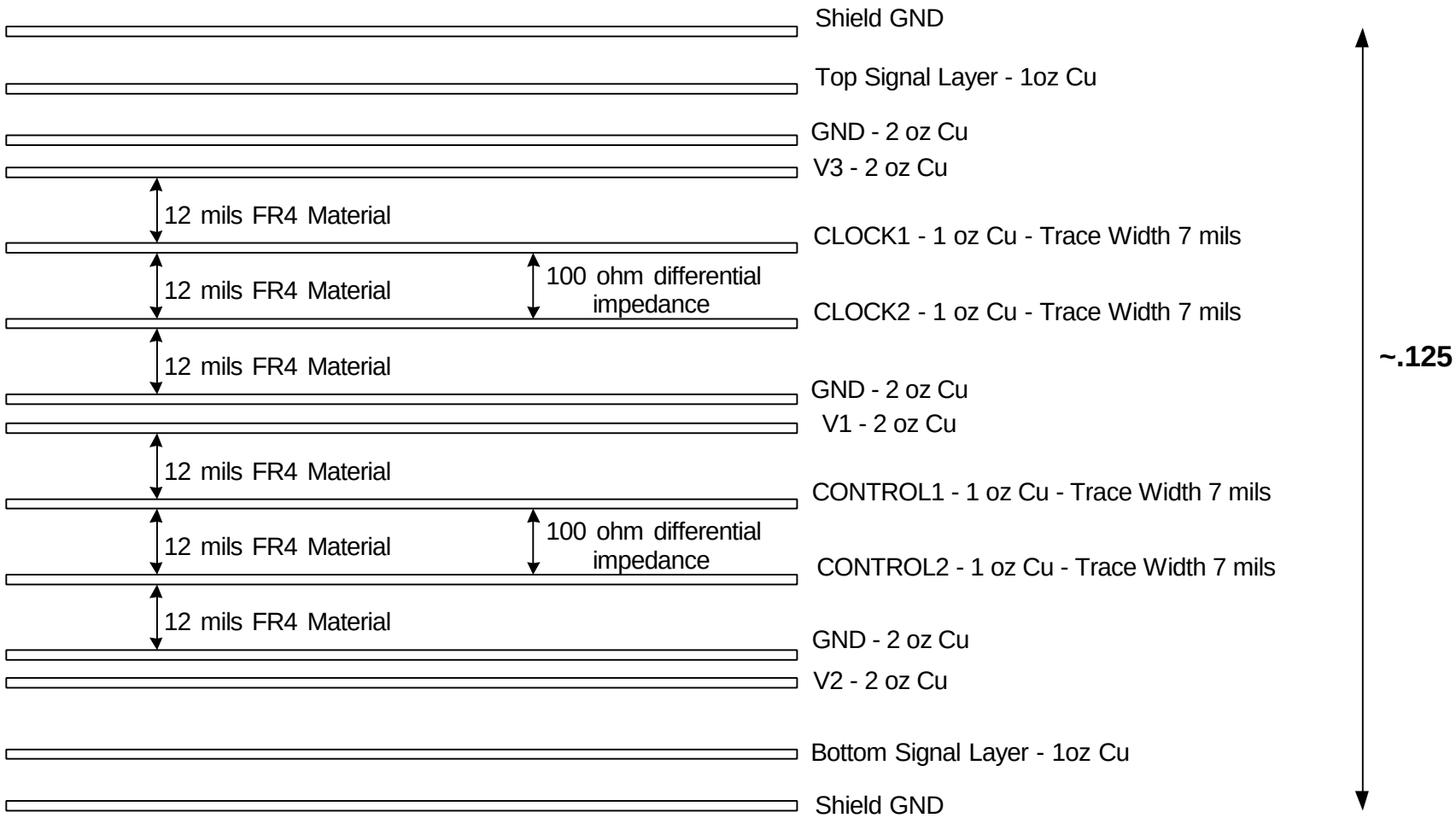


FE Card Pinout

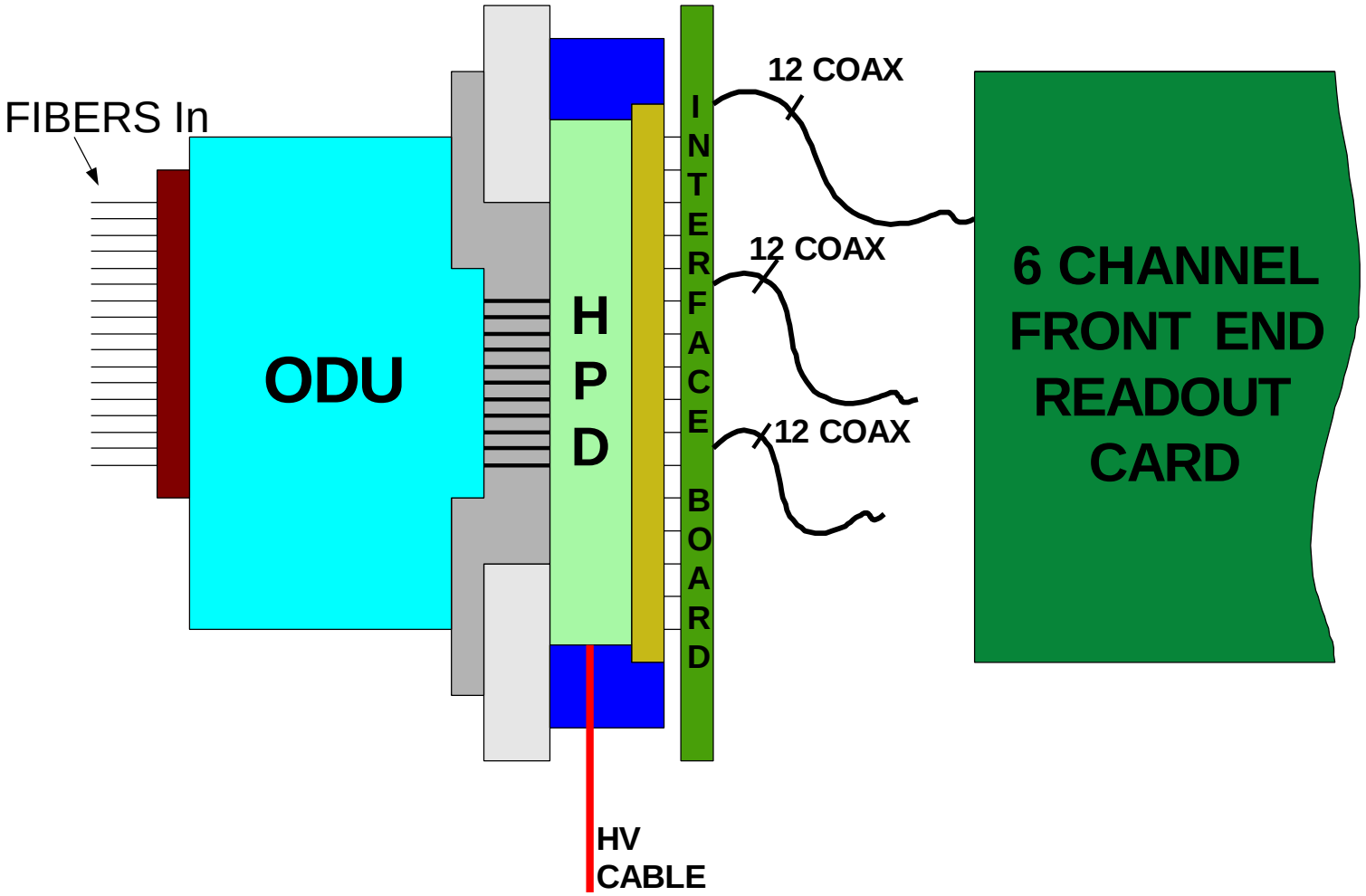
READOUT Card Slot

Pin Number	Row A	Row B	Row C
1	GND	GND	GND
2	V1	V1	V1
3	GND	GND	GND
4	V2	V2	V2
5	GND	GND	GND
6	V3	V3	V3
7	GND	GND	GND
8	MCLK+	D0_CALIB	RESERVED
9	MCLK-	GND	GND
10	GND	GND	TEMP
11	GEO_ADDR(0)	GND	GND
12	GEO_ADDR(1)	GND	RSVD(1)
13	RESET+	GND	RSVD(2)
14	RESET-	GND	SERCLK+
15	BZERO+	GND	SERCLK-
16	BZERO-	GND	SER_DAT

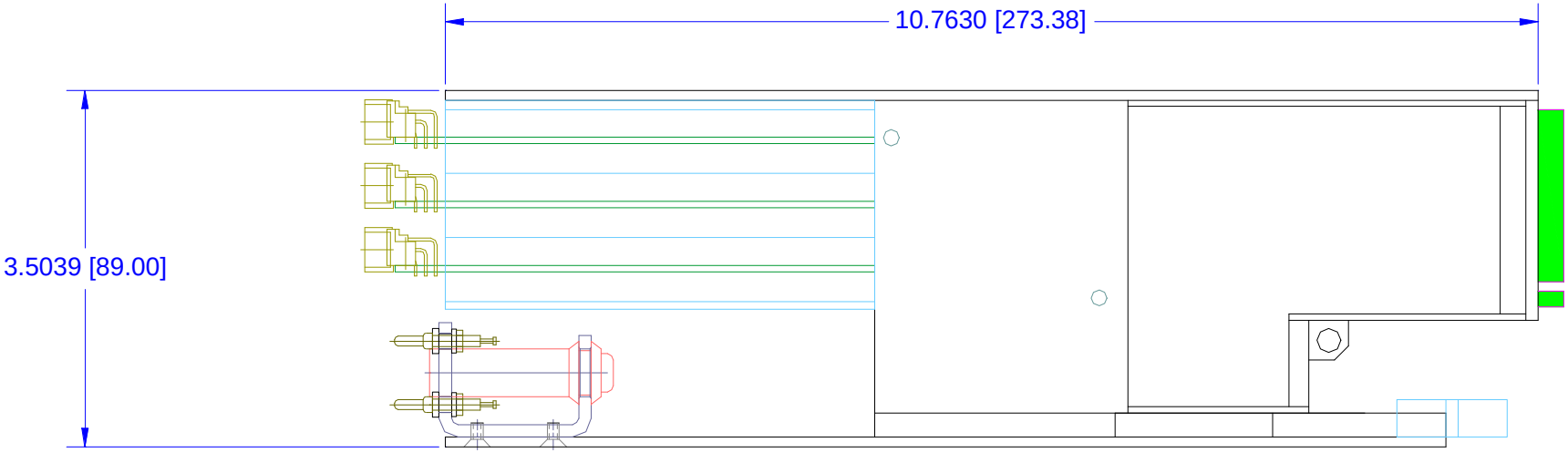
Backplane Stack-up



Readout Module Overview

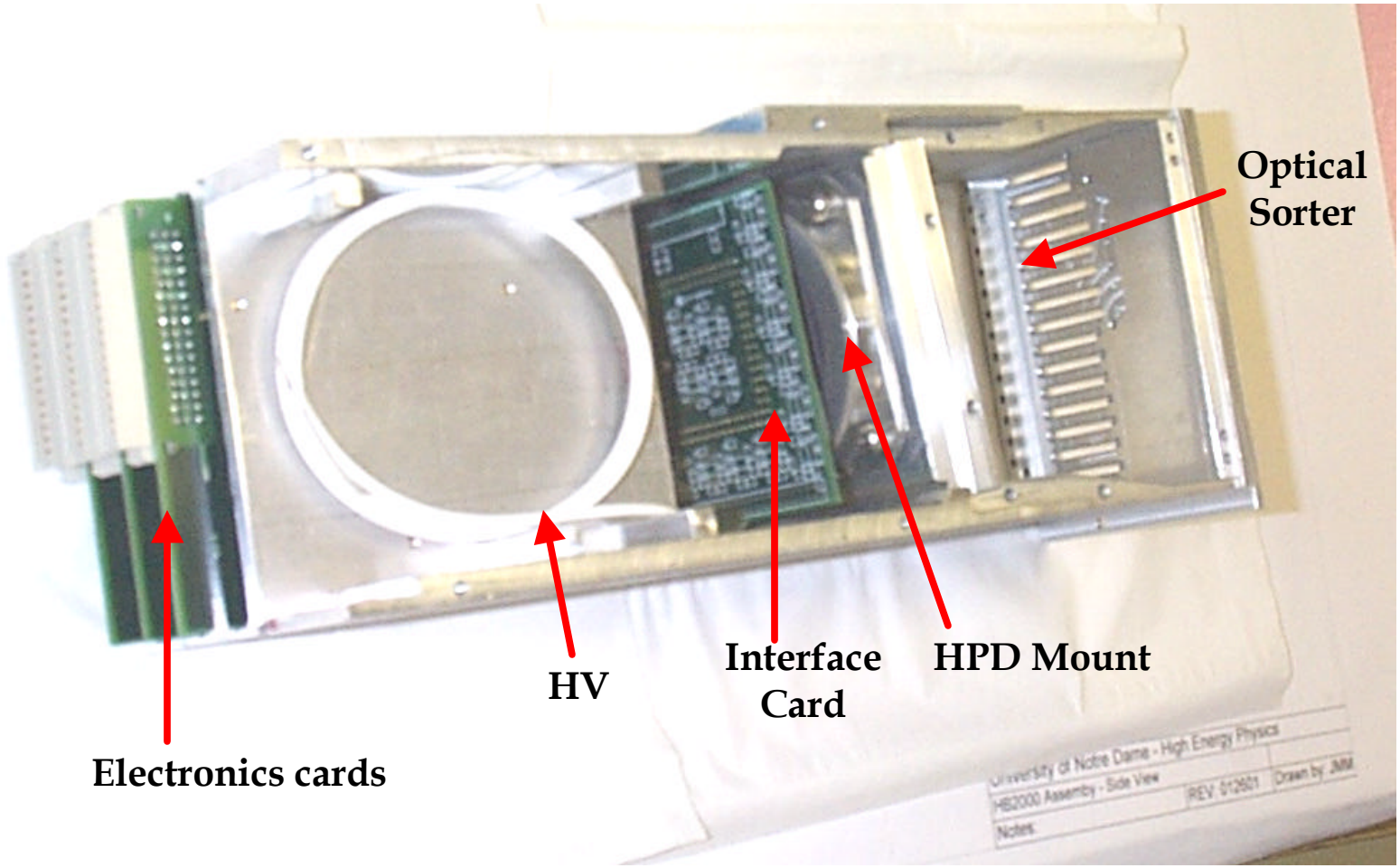


RM-19 Plan View

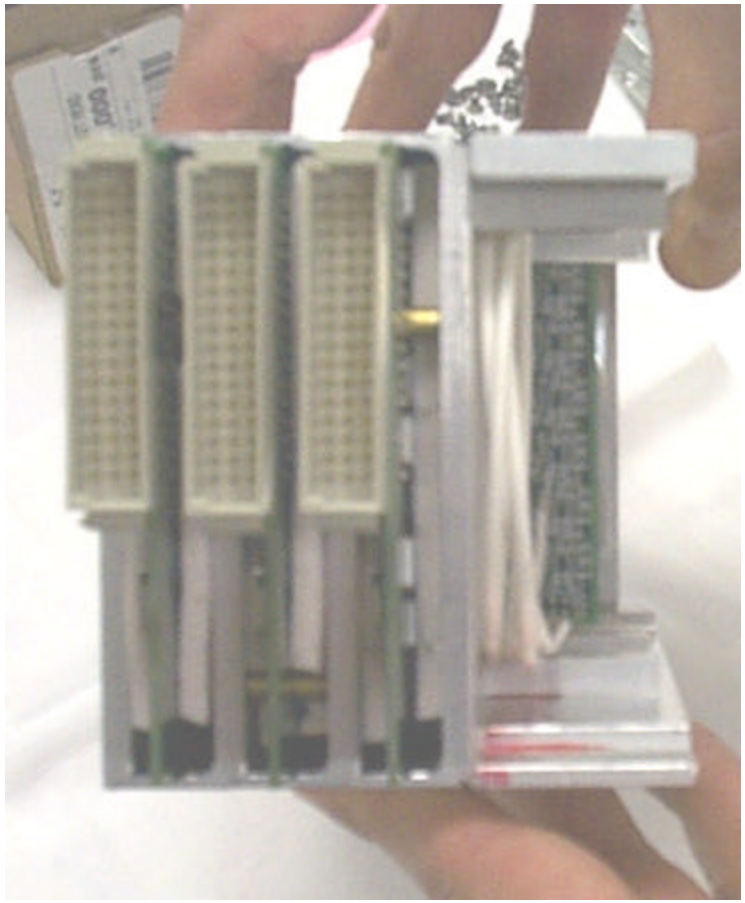


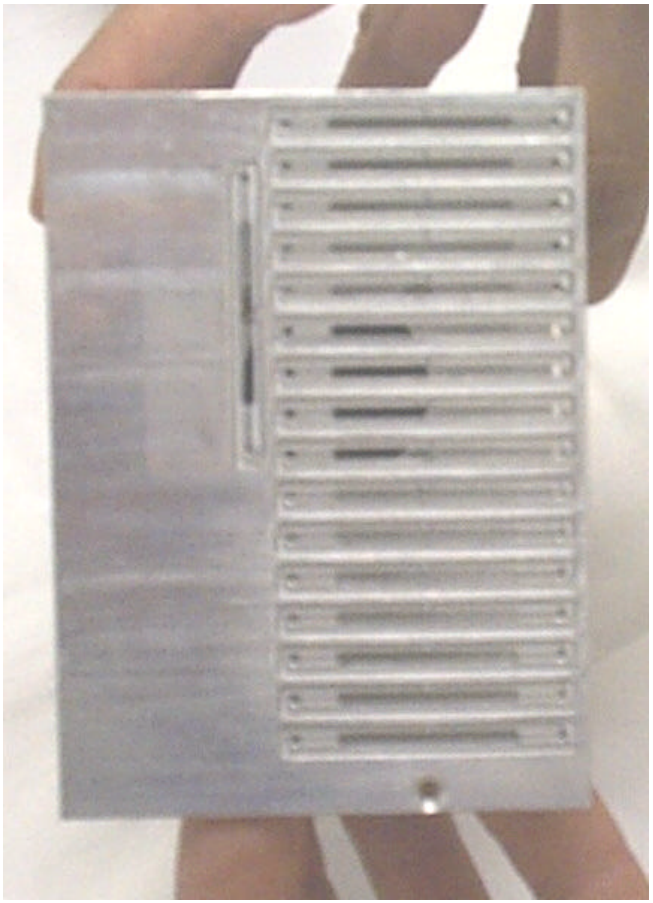
RM19 Sidewall removed

- **The readout module (RM) integrates the HPD, front end electronics, and digital optical drivers.**

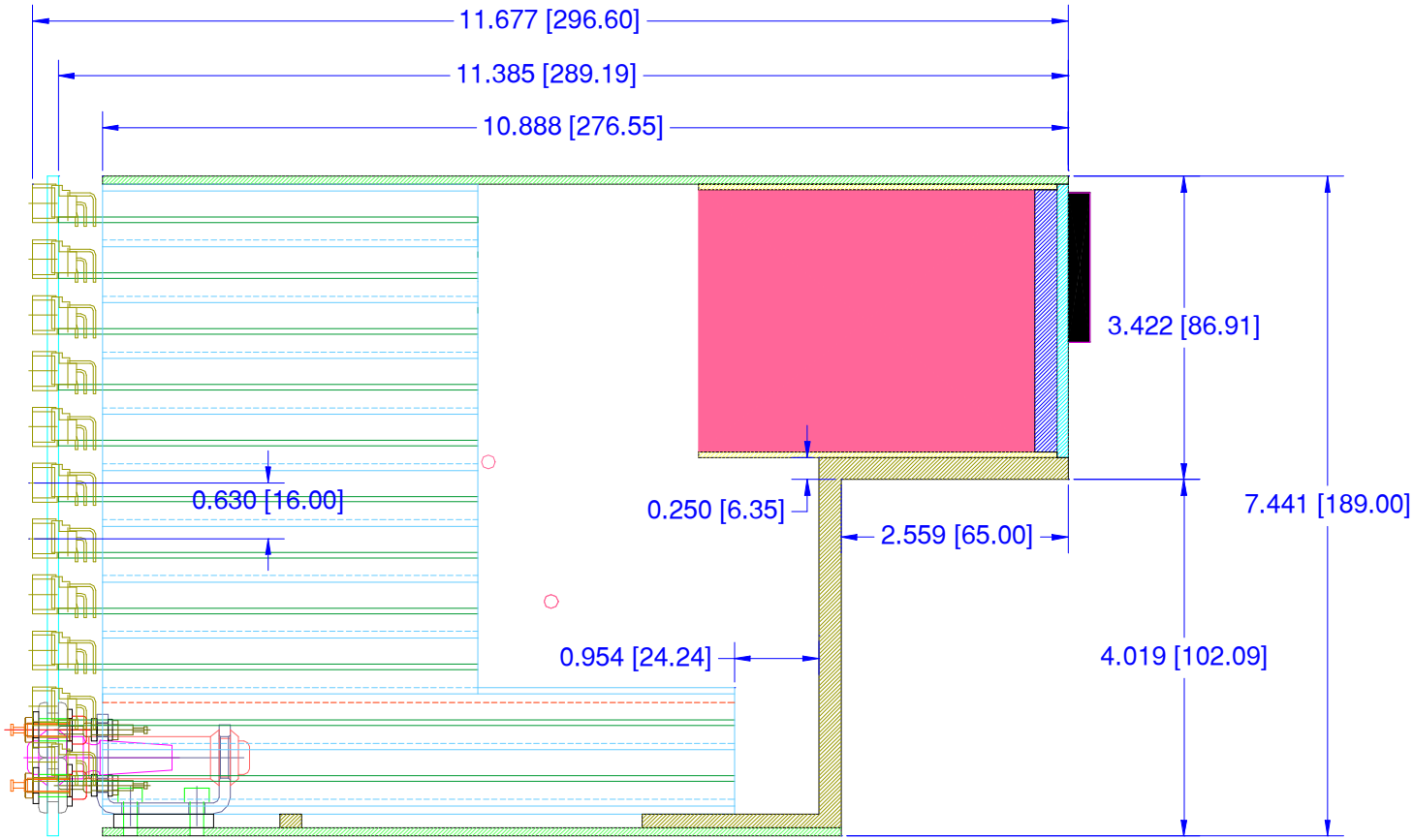


RM19 Rear and Front Views

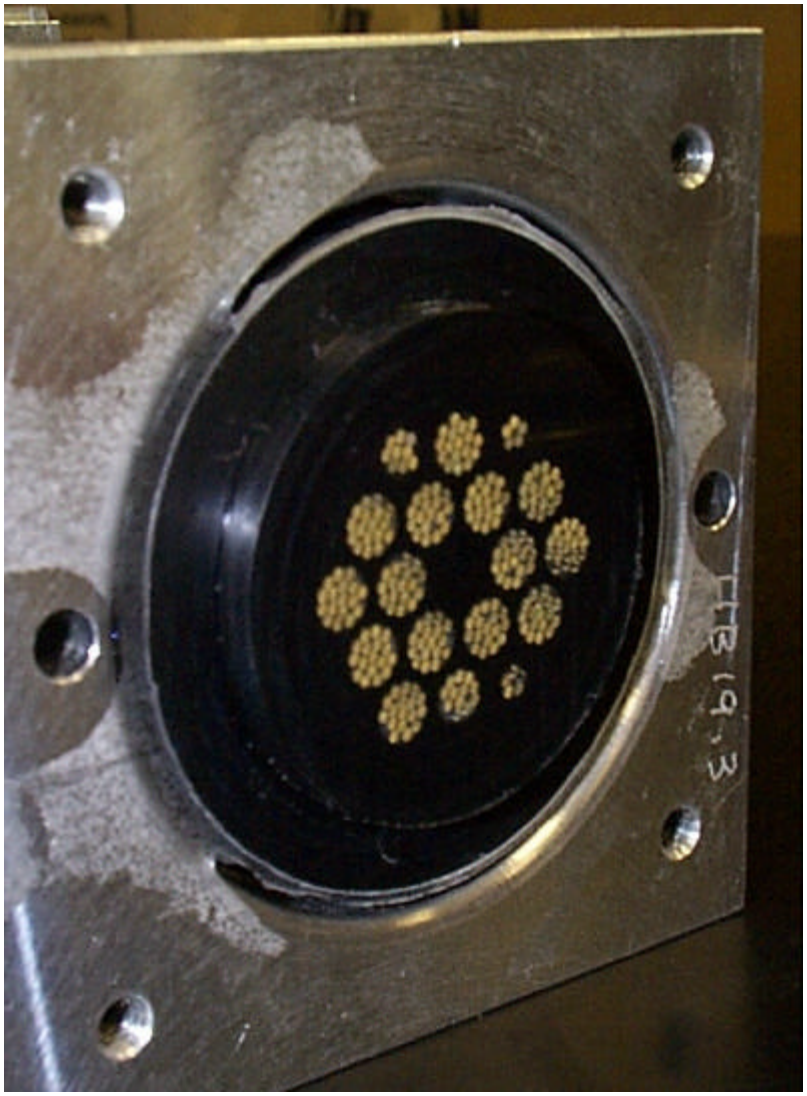




RM-73


11.677 [296.60]
11.385 [289.19]
10.888 [276.55]
3.422 [86.91]
7.441 [189.00]
0.630 [16.00]
0.250 [6.35]
2.559 [65.00]
0.954 [24.24]
4.019 [102.09]

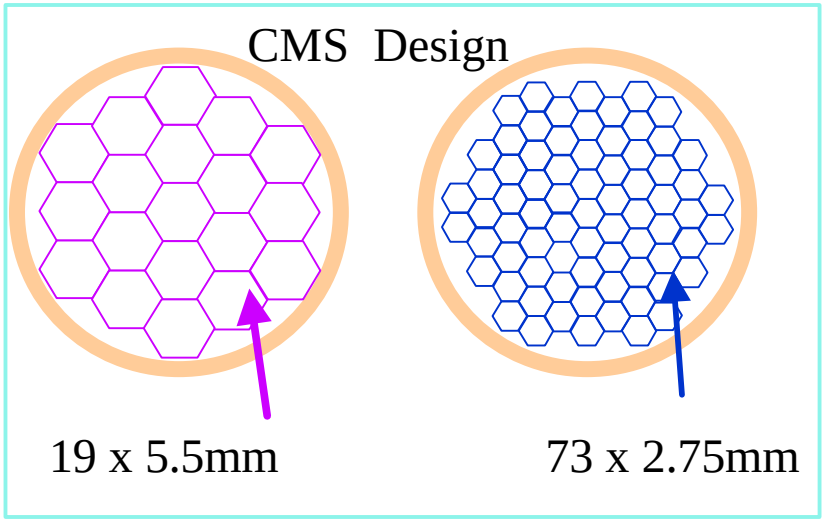
ODU Construction - ‘01



The Hybrid Photodiode (HPD)

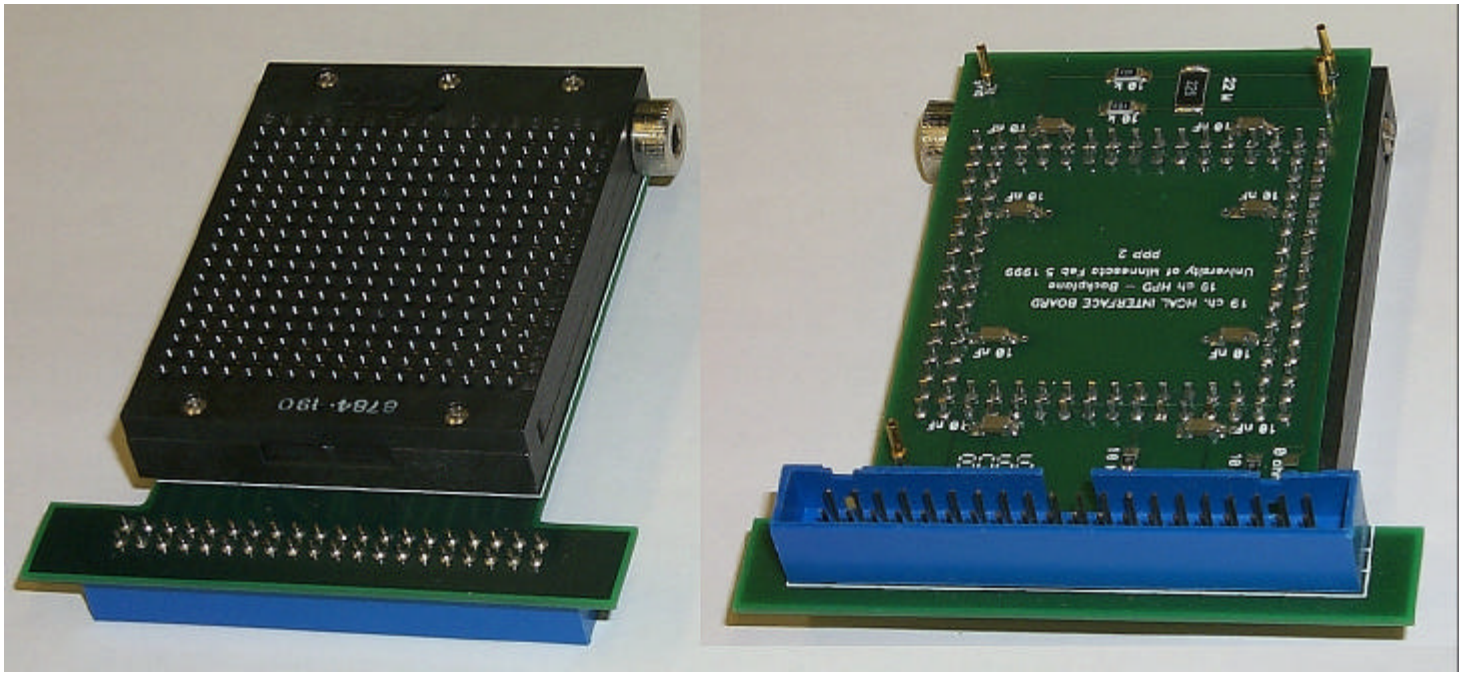
Tube Fabrication by Delft Electronic Products (Netherlands)

Subcontracts: Canberra (Belgium) 22% for diodes
Schott Glass (USA) 8% for fiber optic windows
Kyocera (Japan) 4% for vacuum feedthru/ceramic carrier



- 12 kV across 3.5 mm gap with V_{th} < 3 kV => Gain of 2500
- Silicon PIN diode array, T-type
- Thin (200 μm) with 100 V reverse bias for fast charge (holes) collection

HPD Interface Board

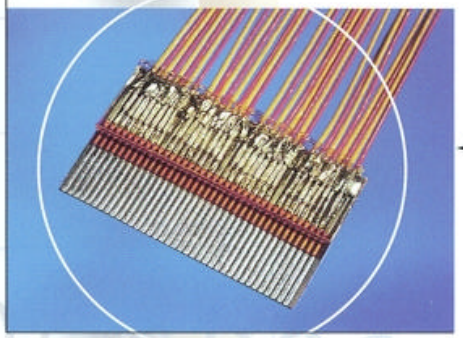


Signal Cable Candidate(1)

PICO-FLEX®

OR USE PICO-FLEX :

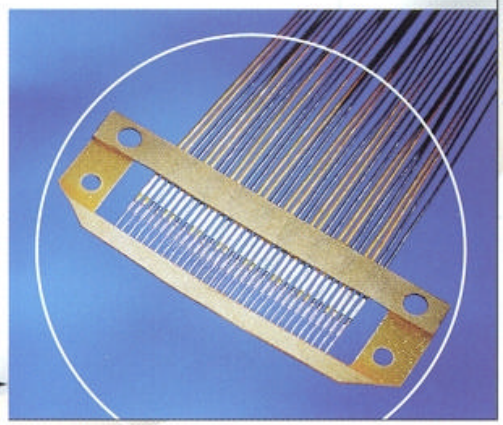
- Mounted in a ZIF connector surface mounted on a PCB.
- Available in 0,5 mm pitch (0,019").
- Compatible with PICO-COAX® AWG 40 to 46 (50 and 100 pF/m, 15 and 30 pF/ft).
- Custom designed versions available on request.



PICO-WELD®

USE PICO-WELD® :

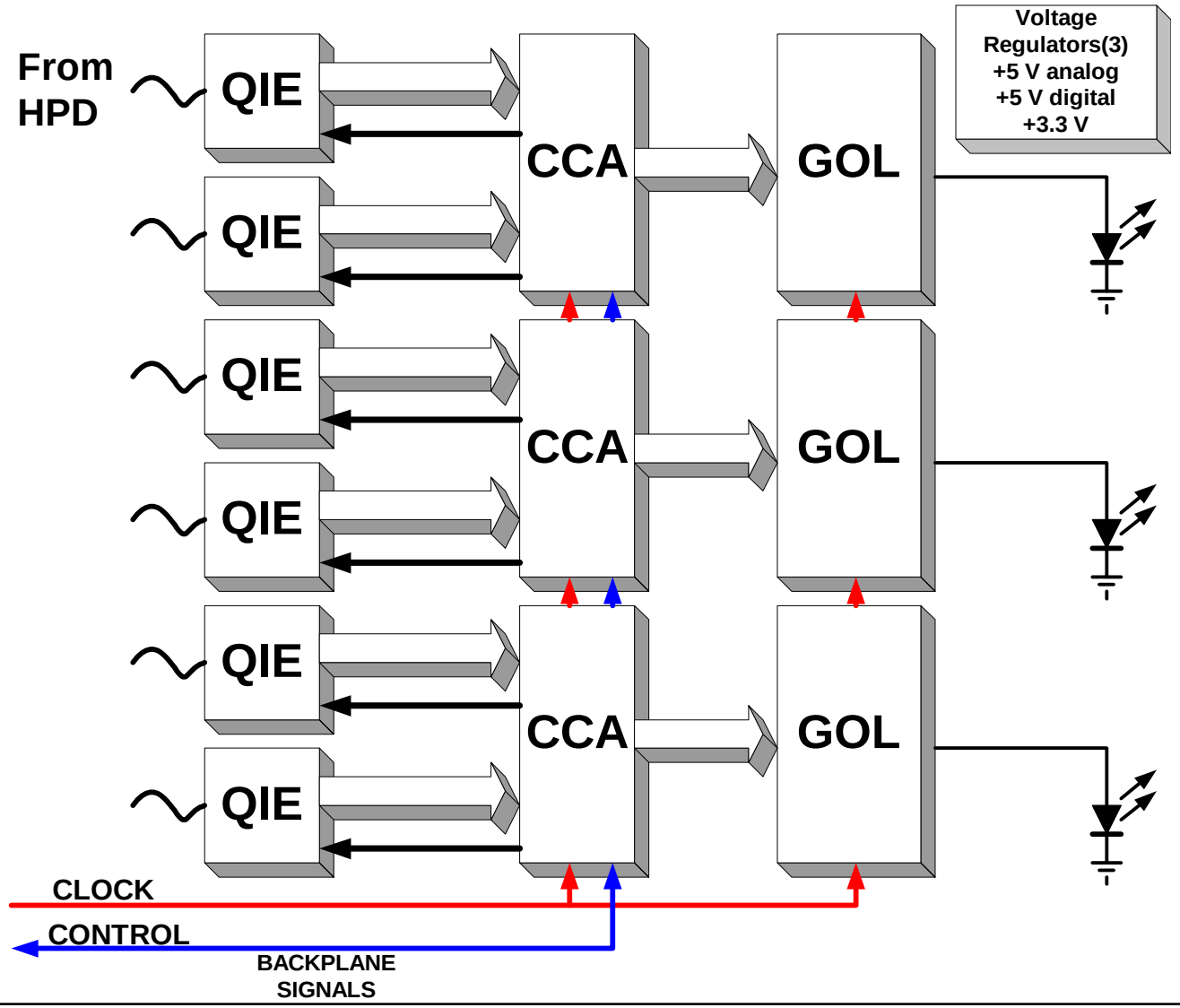
- Solders directly to PC board.
- Maintains alignment of the PICO-COAX® at a constant pitch.
- Hot bar system soldering.
- Available in 32 positions pitch 0,635 mm (0,025").
- Compatible with AWG 40 and 42 (50 and 100 pF/m, 15 and 30 pF/ft).
- Other constructions available on request



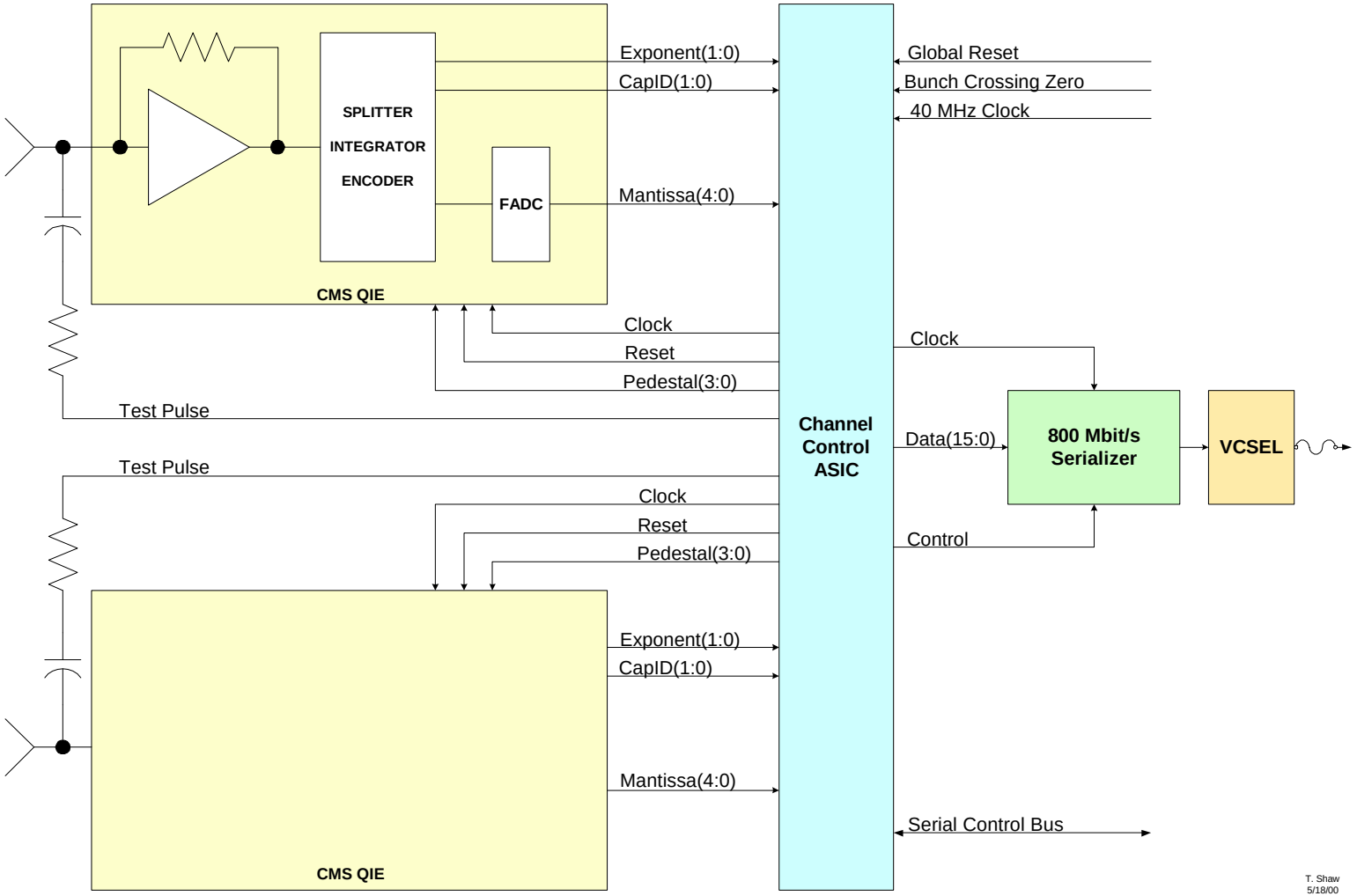
Signal Cable Candidate(2)

GET CABLE/CONNECTOR SPECS

Block Diagram of FE Card



FE Channels



CMS QIE Solution

QIE Description

QIE

Charge Integrator Encoder

4 stage pipelined device (25ns per stage)

- charge collection
- settling
- readout
- reset

Inverting (HPDs) and Non-inverting (PMTs) Inputs

Internal non-linear Flash ADC

Outputs

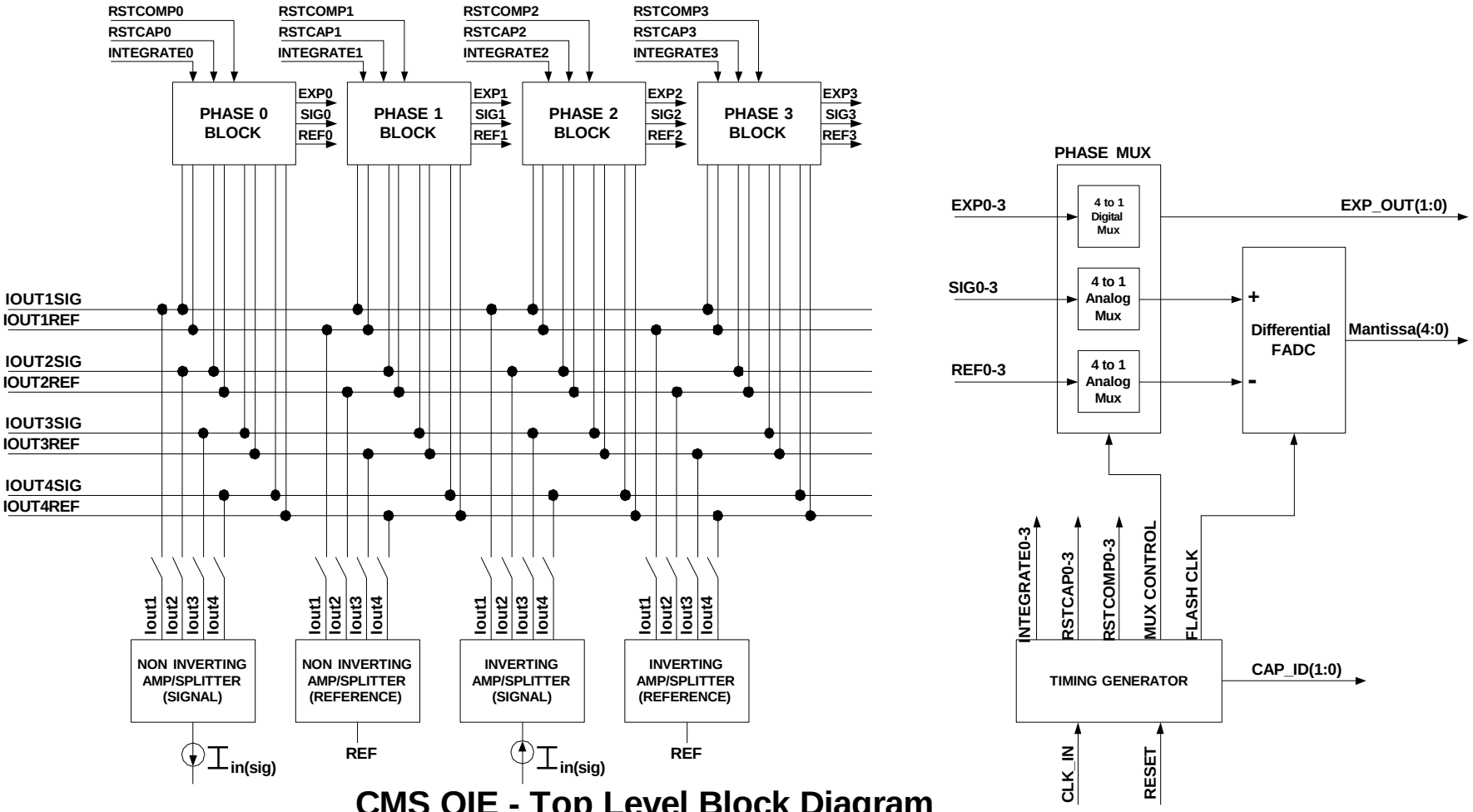
- 5 bit mantissa
- 2 bit range exponent
- 2 bit Cap ID

QIE Specification

QIE Design Specifications

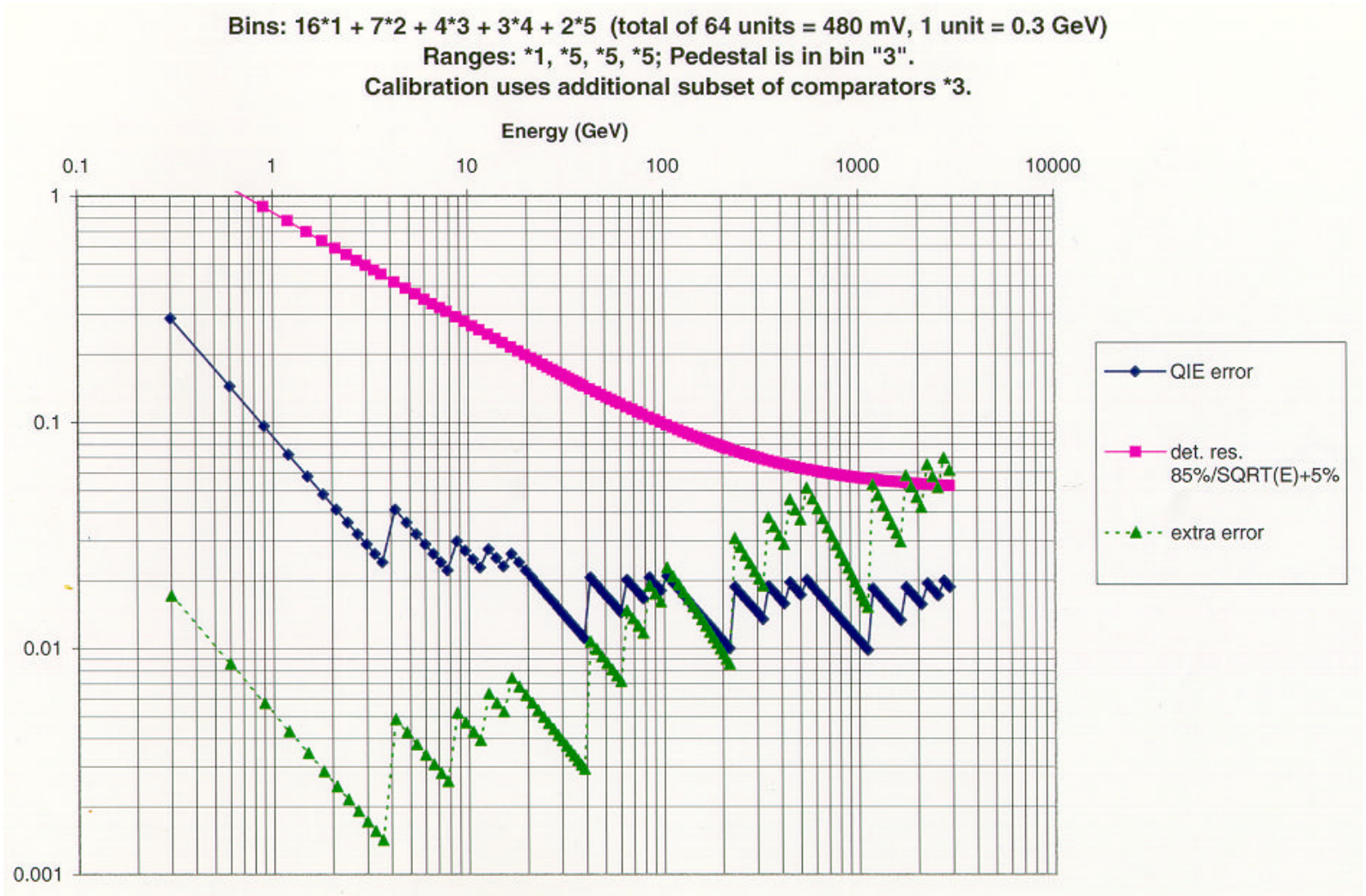
- Clock > 40 MHz
- Must have inverting and non-inverting inputs
- Charge sensitivity of lowest range – 1fC/LSB
  - In Calibration Mode 1/3 fC/LSB
- Maximum Charge – 9670 fC/25ns
- 4500 electrons rms noise
- FADC Differential Non-Linearity < .05 LSBs

QIE Functional Block Diagram – Top Level



CMS QIE - Top Level Block Diagram

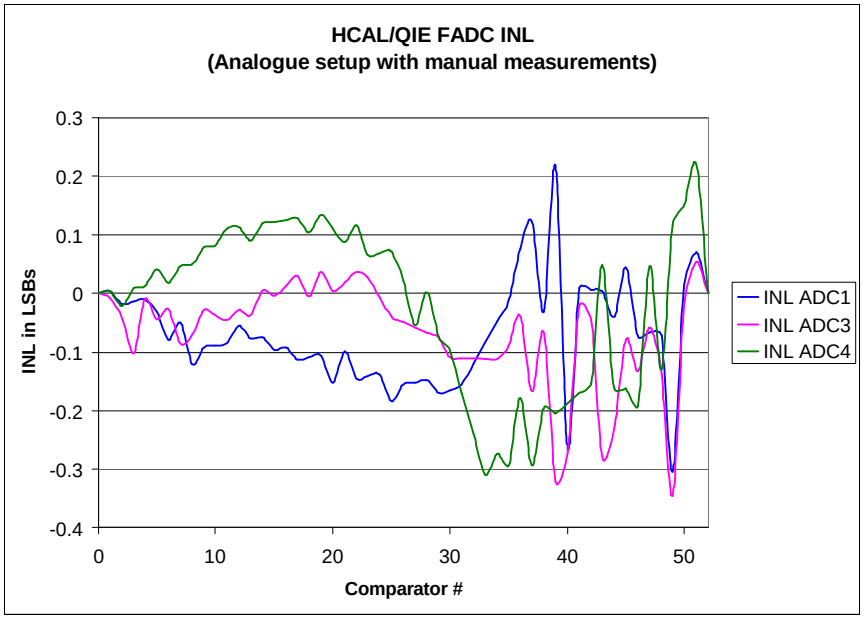
FLASH ADC Quantization

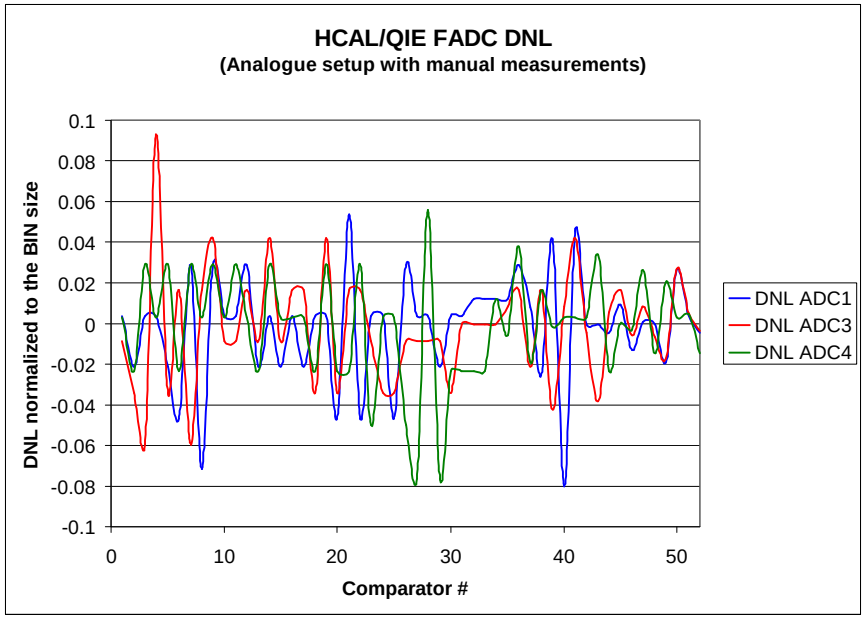


QIE Status

QIE ASIC

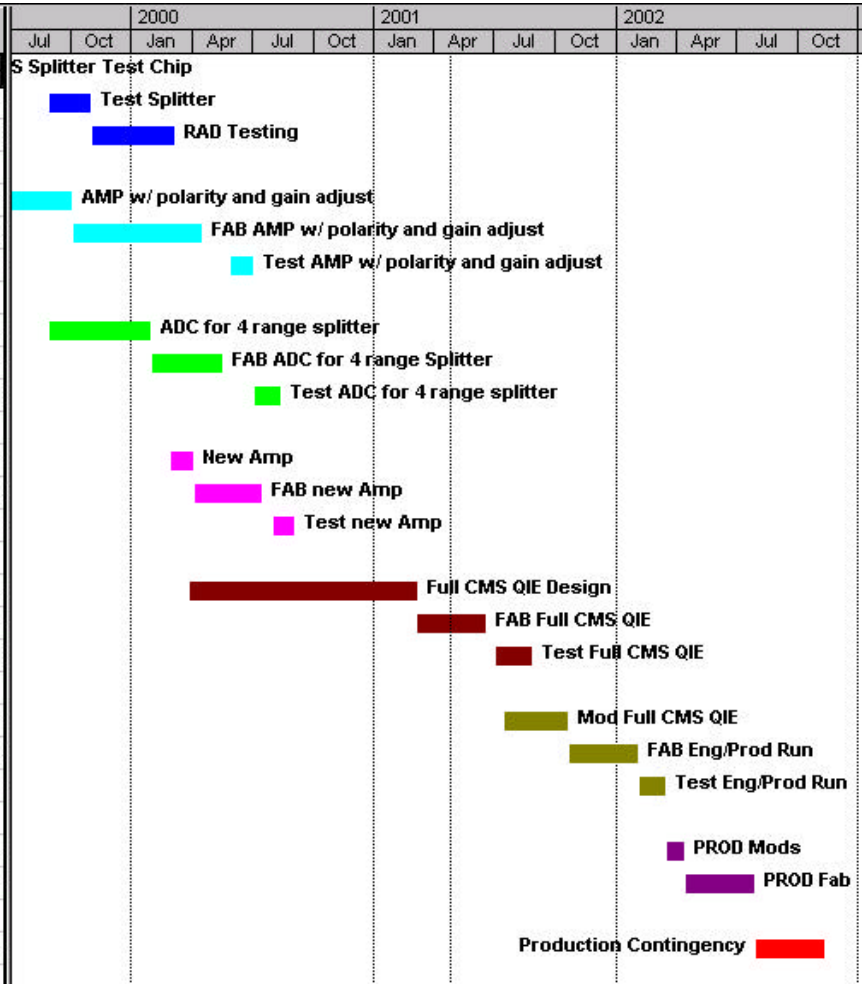
- Current splitter design submitted and tested
- Input amplifier with polarity and gain adjust submitted and tested
- Non-linear Flash ADC design submitted and tested
- Full design submitted – back mid to late June ‘01



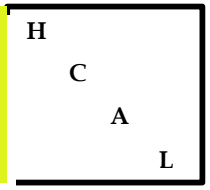


QIE Schedule

Task Name	Start	Finish	Duration
AMS splitter test chip	Mon 11/2/98	Fri 4/30/99	130 days
Test Splitter	Mon 8/30/99	Fri 10/29/99	45 days
RAD Testing	Mon 11/1/99	Fri 3/3/00	90 days
AMP w/ polarity and gain adjust	Mon 6/28/99	Fri 10/1/99	70 days
FAB AMP w/ polarity and gain adjus	Mon 10/4/99	Fri 4/14/00	140 days
Test AMP w/ polarity and gain adjus	Mon 5/29/00	Fri 6/30/00	25 days
ADC for 4 range splitter	Mon 8/30/99	Fri 1/28/00	110 days
FAB ADC for 4 range Splitter	Tue 2/1/00	Mon 5/15/00	75 days
Test ADC for 4 range splitter	Mon 7/3/00	Fri 8/11/00	30 days
New Amp	Mon 2/28/00	Fri 3/31/00	25 days
FAB new Amp	Mon 4/3/00	Fri 7/14/00	75 days
Test new Amp	Mon 7/31/00	Fri 9/1/00	25 days
Full CMS QIE Design	Mon 3/27/00	Mon 3/5/01	246 days
FAB Full CMS QIE	Mon 3/5/01	Fri 6/15/01	75 days
Test Full CMS QIE	Mon 7/2/01	Fri 8/24/01	40 days
Mod Full CMS QIE	Mon 7/16/01	Fri 10/19/01	70 days
FAB Eng/Prod Run	Mon 10/22/01	Fri 2/1/02	75 days
Test Eng/Prod Run	Mon 2/4/02	Fri 3/15/02	30 days
PROD Mods	Mon 3/18/02	Fri 4/12/02	20 days
PROD Fab	Mon 4/15/02	Fri 7/26/02	75 days
Production Contingency	Mon 7/29/02	Fri 11/8/02	75 days



Channel Control ASIC



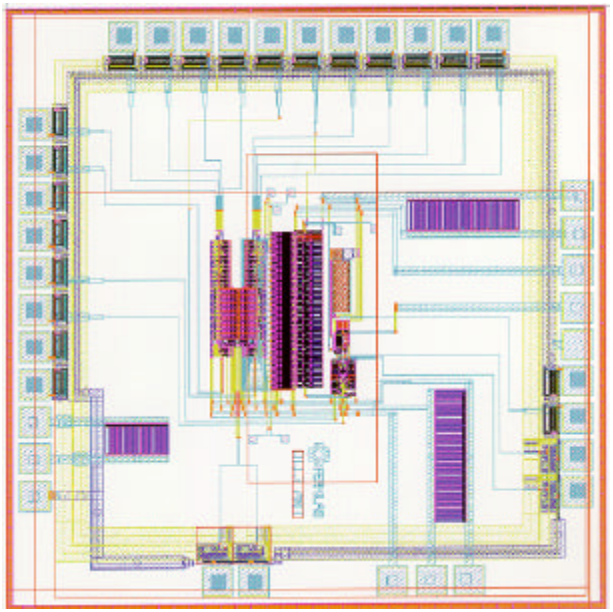
The CCA provides the following functions:

- The processing and synchronization of data from two QIEs,
- The provision of phase-adjusted QIE clocking signals to run the QIE charge integrator and Flash ADC,
- Checking of the accuracy of the Capacitor IDs, the Cap IDs from different QIEs should be in synchronization,
- The ability to force the QIE to use a given range,
- The ability to set Pedestal DAC values,
- The ability to issue a test pulse trigger,
- The provision of event synchronization checks – a crossing counter will be implemented and checked for accuracy with every beam turn marker,
- The ability to send a known pattern to the serial optic link,
- The ability to “reset” the QIE at a known and determined time,
- And, the ability to send and report on any detected errors at a known and determined time.

CCA Status

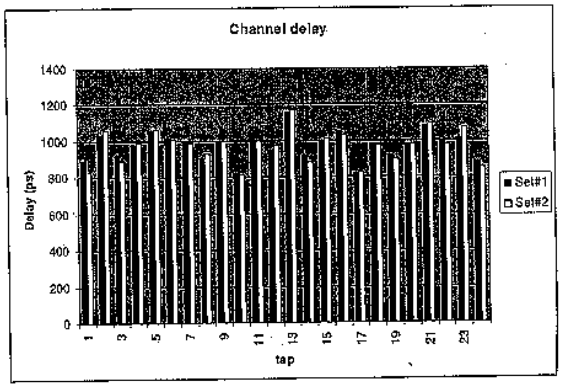
Channel Control ASIC

- DLL for timing control submitted and tested
- 1ns multiplexer design submitted and tested
- Serial Interface design submitted and tested



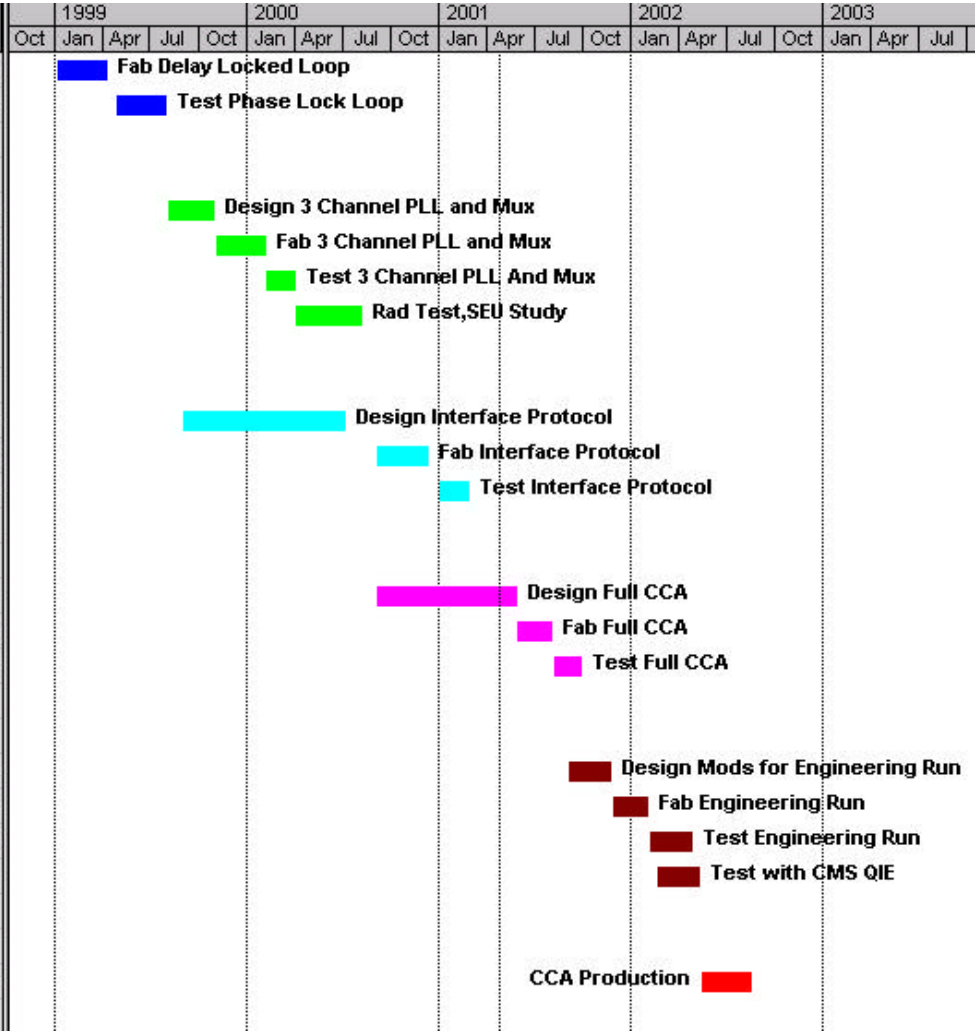
Measured delays vs. tap

- Average delay : 972p STD : 77ps
- Min delay : 810p
- Max delay : 1170p



CCA Schedule

Task Name	Start	Finish	Duration
Fab Phase Locked Loop	Mon 1/4/99	Fri 4/9/99	70 days
Test Phase Lock Loop	Mon 4/26/99	Fri 7/30/99	70 days
Design 3 Channel PLL and	Mon 8/2/99	Fri 10/29/99	65 days
Fab 3 Channel PLL and Mu	Mon 11/1/99	Fri 2/4/00	70 days
Test 3 Channel PLL And M	Mon 2/7/00	Fri 3/31/00	40 days
Rad Test, SEU Study	Mon 4/3/00	Fri 8/4/00	90 days
Design Interface Protocol	Tue 8/31/99	Mon 7/3/00	220 days
Fab Interface Protocol	Mon 9/4/00	Fri 12/8/00	70 days
Test Interface Protocol	Mon 1/1/01	Fri 2/23/01	40 days
Design Full CCA	Mon 9/4/00	Fri 5/25/01	190 days
Fab Full CCA	Mon 5/28/01	Fri 8/3/01	50 days
Test Full CCA	Mon 8/6/01	Fri 9/28/01	40 days
Design Mods for Engineeri	Mon 9/3/01	Fri 11/23/01	60 days
Fab Engineering Run	Mon 11/26/01	Fri 2/1/02	50 days
Test Engineering Run	Mon 2/4/02	Fri 4/26/02	60 days
Test with CMS QIE	Mon 2/18/02	Fri 5/10/02	60 days
CCA Production	Mon 5/13/02	Fri 8/16/02	70 days



QIE/CCA Process Reliability

AMS 0.8u BiCMOS Process (QIE)

Early Failure rate 0.05 - 0.2%; can be reduced to a few ppm by burn-in

Predicted MTTF (25 sqmm, 55 C) is 1.67E8 hours

Expect less than 1 QIE failure per year

HP/Agilent 0.5u CMOS

Well established Commercial Process

GOL Design Specifications

Synchronous (constant latency)

Transmission speed

- **fast: 1.6 Gbps , 32 bit data input @ 40 MHz**
- **slow: 0.8 Gbps , 16 bit data input @ 40 MHz**

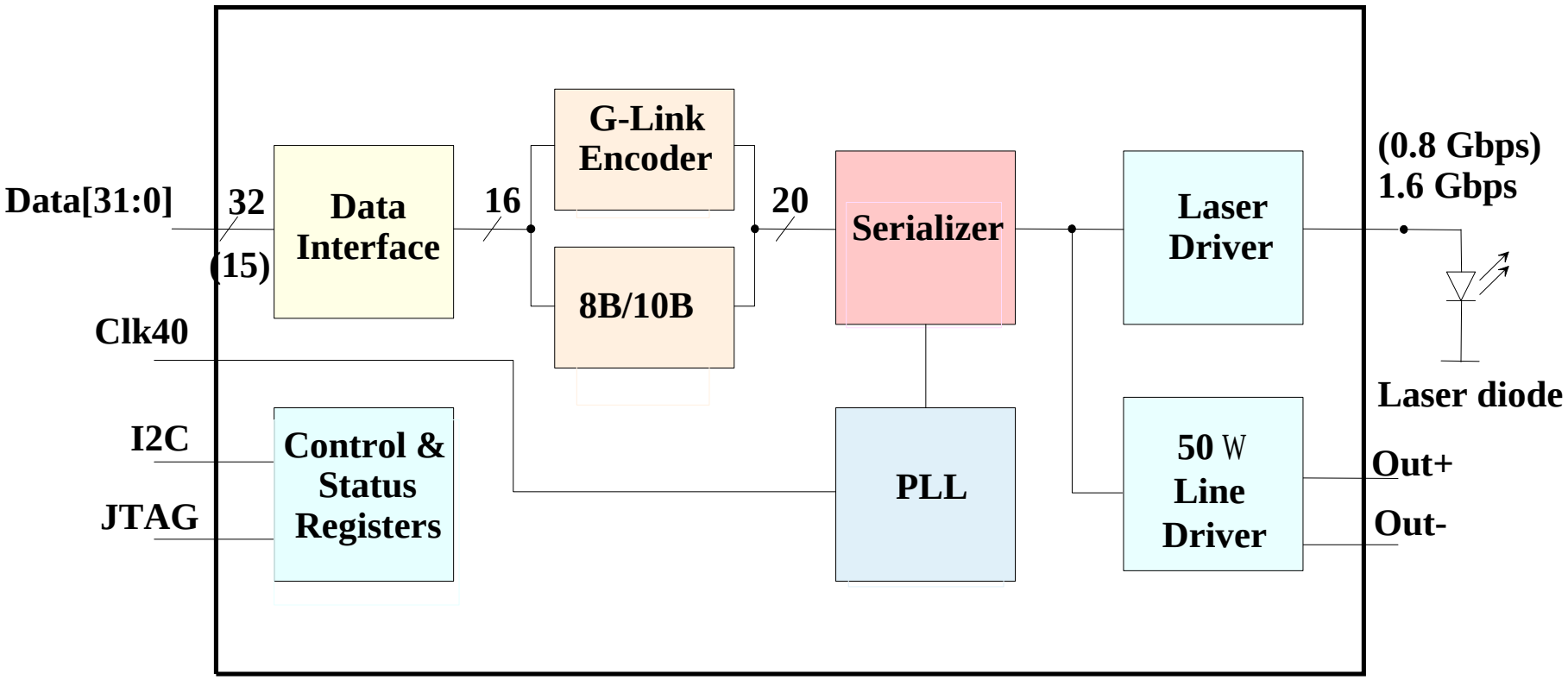
Two encoding schemes

- **G-Link**
- **Fiber channel (8B/10B)**

Interfaces for control and status registers

- **I2C**
- **JTAG**

Gigabit link (G-Link, 8B/10B optional)



GOL Radiation hardness

Deep submicron (0.25 um) CMOS

Enclosed CMOS transistors

Triple voting in state machines

Up-sizing of PLL components

Auto-error correction in Config. registers

Single Event Upsets

- Can we extrapolate for LHC?

CMS Environment	Pixel R = 4 – 20cm	Endcap ECAL R = 50 – 130cm	Tracker R = 65-120cm	Cavern R = 700 – 1200cm
Error/(chip hour)	$1.4\ 10^{-2}$	$1.9\ 10^{-4}$	$8.4\ 10^{-5}$	$3.1\ 10^{-8}$
#chips for one error each hour!	71	5.3K	12K	32M

GOL Status

- **Bit error rate test in the 800Mbit/s G-Link mode: 20 hours error free transmission (external laser driver).**
- **Bit error rate test in the 1.6Gbit/s 8B/10B mode: 13 hours error free transmission (external laser driver).**
- **I2C interface successfully tested.**
- **JTAG interface successfully tested.**

- **Need to understand and fix jitter problem on internal laser driver. This will be fixed in the next submission (April '01).**

VCSEL Selection

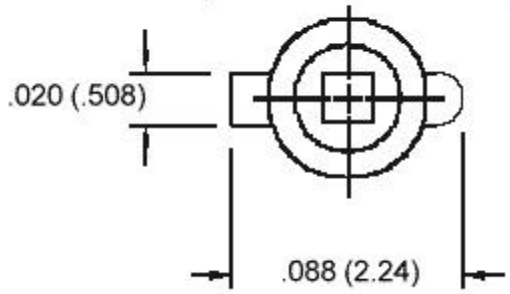
HFE4086-001

VCSEL Components, Data Communications, Flat Window Pillpack, Unattenuate optics, no back monitor photodiode

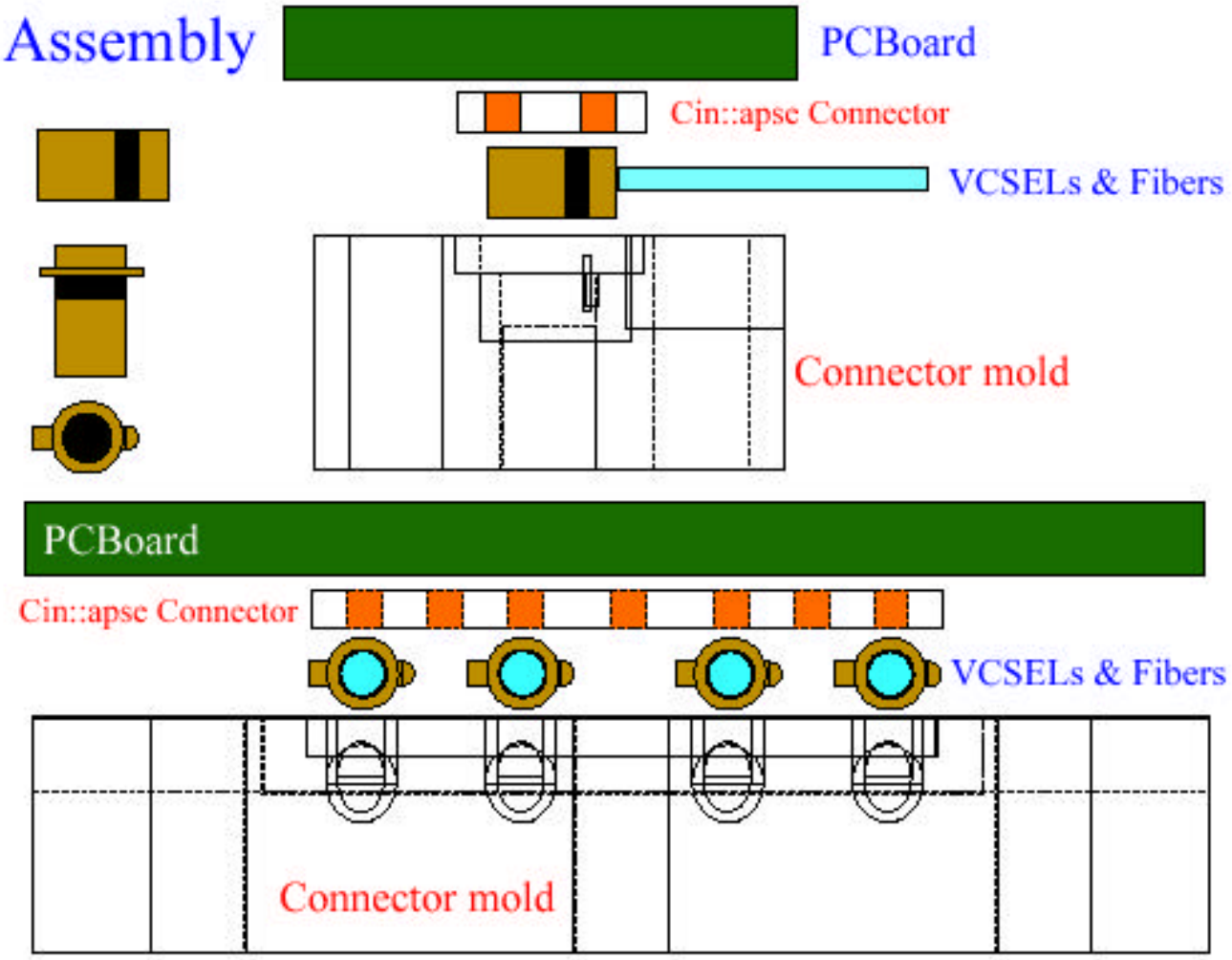
FEATURES

- Designed for drive currents between 5 mA and 15 mA
- Optimized for low dependence of electrical properties over temperature
- High speed > 1 Ghz
- Miniature flat-window, pill-pack package

MOUNTING DIMENSIONS (for reference only): in./(mm)



VCSEL Mechanics



Rad Tolerant Voltage Regulator

Developed by ST Microelectronics

Specified by CERN RD49

Shown to be Rad Hard

Presently fixing overvoltage protection

Prepreduction parts due June 2001

Production parts late 2001??

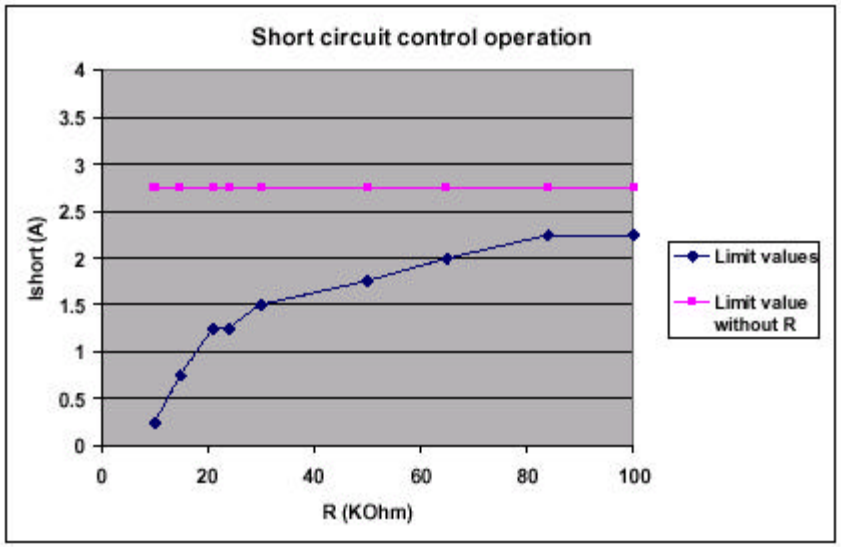
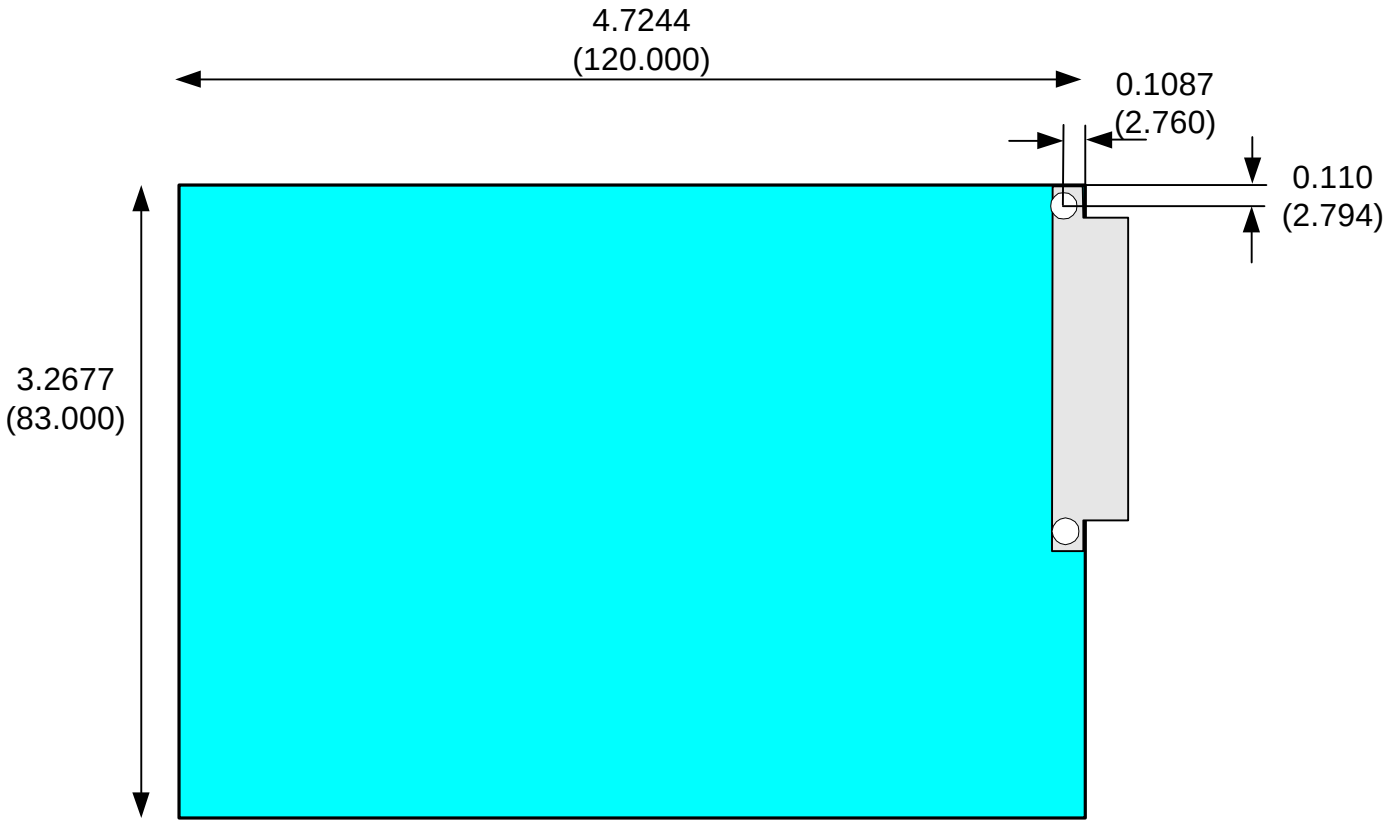
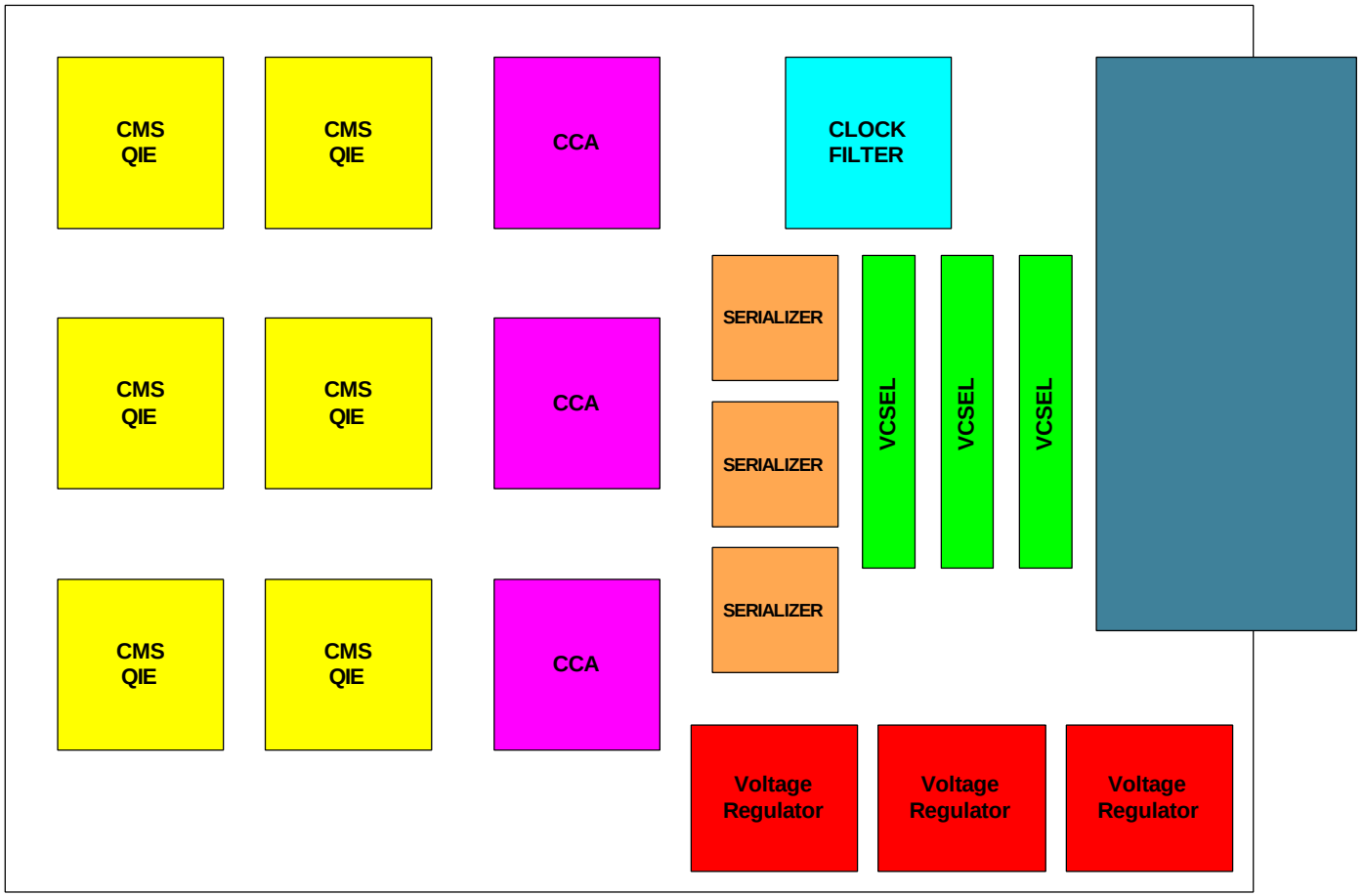


Fig. 7: Tuning of the maximum output current in a 2nd edition prototype regulator (version 2.5 V).

Readout Card Dimension

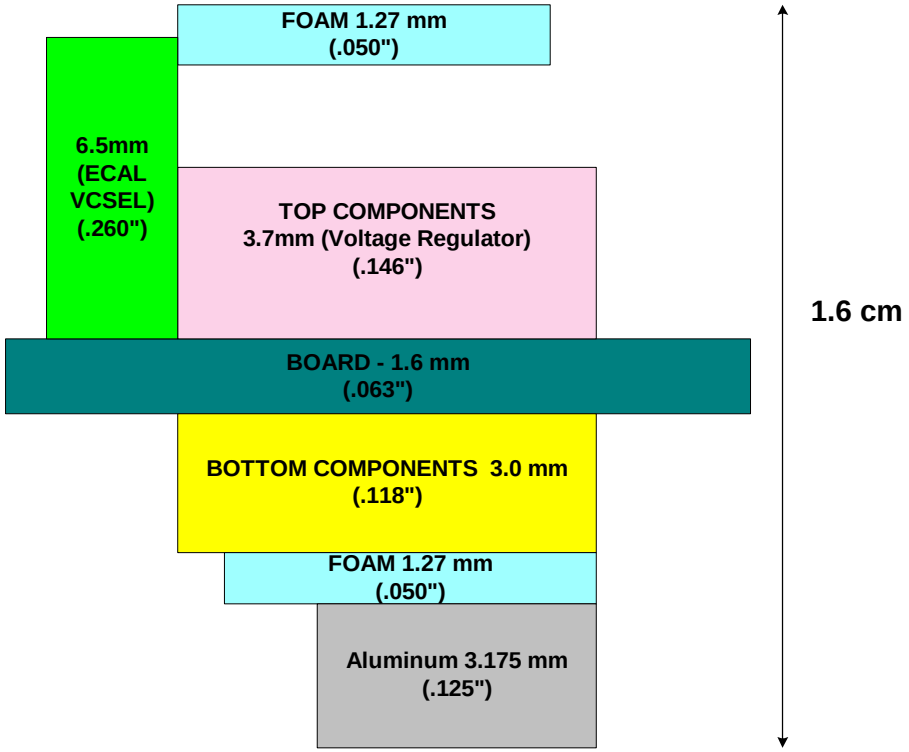


FE Card Component Area



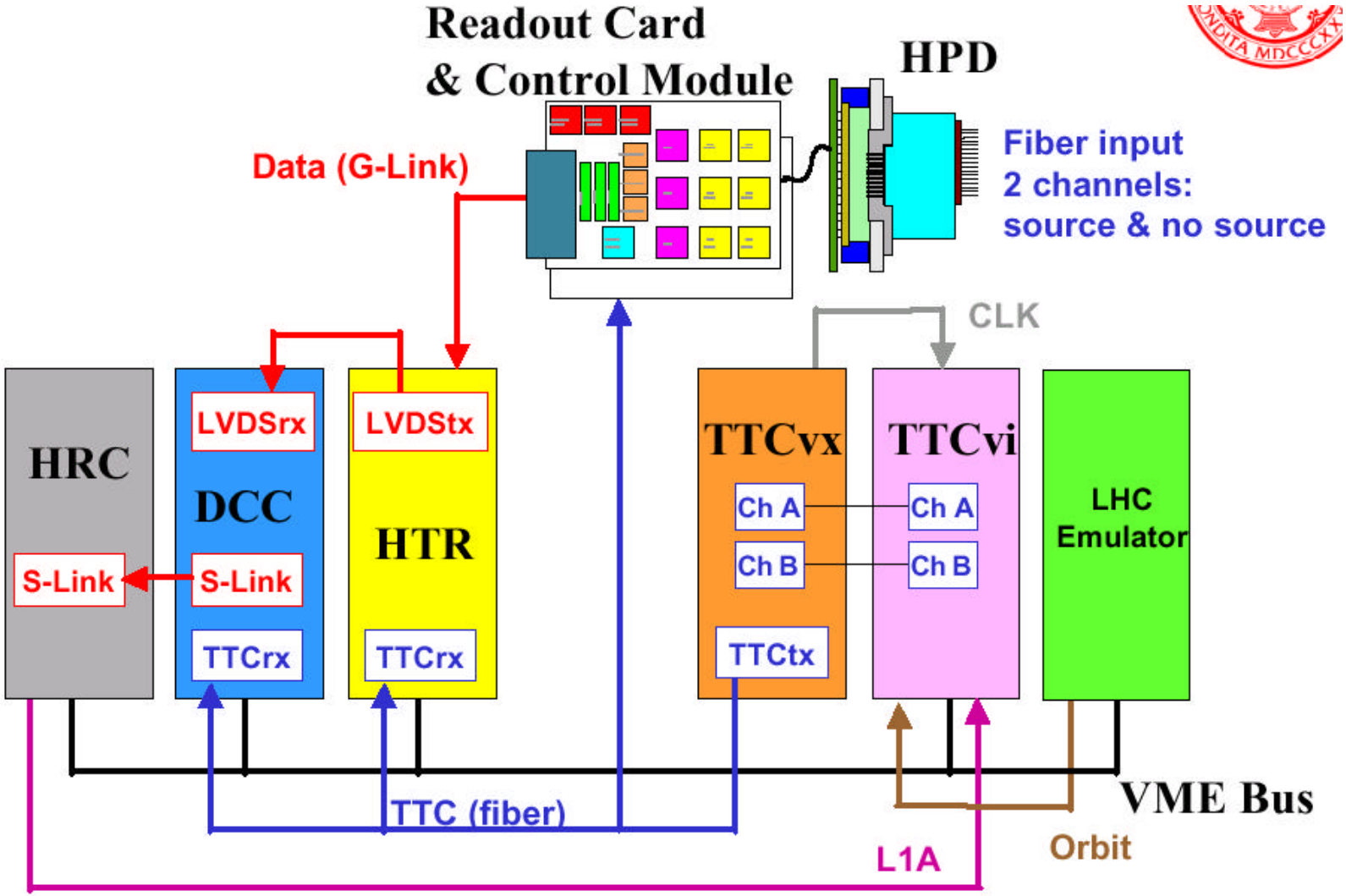
Readout Card Component Height

Goal is 1.6 cm stack



Geometric Space For Components

Plan for FE/HTR Integration



Summary

FE/DAQ integration planned for this fall

- **2 channel FE card**
  - 2 QIEs
  - Commercial G-Link (@800 Mb/s)
- **6U HTR card**
- **9U DCC module**

Next – ready for summer 2002 test beam

- **6 channel FE card**
  - 6 QIEs
  - Rad hard Voltage Regulator
  - GOL (8B/10B Encoding @1.6Gb/s)
  - Custom VCSEL package
  - CCA